DesignCon2002

Leading Edge Communication Design Conference

A New Method For Simultaneously Measuring And Analyzing PLL Transfer Function And Noise Processes

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Abstract

Phase Locked Loop (PLL) technology has received a wide range of applications in modern datacom, telecom, wireless communications, as well as computer related microprocessor, data bus, video and audio ICs. As the speed of microprocessors approach and exceed 1 GHz, and the serial data transmission rate approaches and exceeds 1 Gb/s, the difficulties and complexities of designing and manufacturing a PLL at these speeds become severe. An important problem in PLL design and manufacture is to simulate, measure, and verify its loop response and noise processes in order to achieve goals of good time and frequency domain responses, as well as good noise and jitter performance. In this paper, we will introduce our new methodology that is capable of simulating and measuring a PLL loop response and noise/jitter processes in an integrated manner. Key characteristics for a PLL, such as loop response, jitter/noise processes (in both time and frequency domain), locations of poles/zeros, Bode plots, root locus; and key parameters of damping factor, natural frequency, lock time/range, pull-in pull-out range, can be simulated and measured concurrently. This method bridges the gap between PLL design, debug, verification, and manufacture, and it will help to shorten the time from concept to product delivery.

Author Biography

Dr. Li is currently the Chief Technology Officer (CTO) of Wavecrest. He has many years experiences in SI related measurement instrumentation and analysis algorithms/tools. Prior joining Wavecrest, Dr. Li had worked in both industry and academic institutions. Dr. Li is experienced in measurement system architecture, hardware, software, performance, and accuracy. He also has experiences in modeling high energy astrophysical objects, and astrophysical data analysis tools. Dr. Li has a BS in physics from University of Science and Technology of China, a MSE in electrical engineering and a Ph.D. in physics from University of Alabama in Huntsville. He did his Post Dr. at University of California, Berkeley.

Mr. Wilstrup is a corporate consultant at Wavecrest. His present interests are SI simulation and analysis, signal and noise analysis methods and analog circuits. He holds four patents and has six patents pending in the instrumentation area. He studied mathematics and physics at the University of Minnesota.

1.) Introduction

The Phase Locked Loop (PLL) has been widely used in modern data communication, telecommunication, and computer systems. The PLL itself is a complicated electrical feedback system. Its functionality is to provide clean and stable clock output that will be used by the other parts of the system. A PLL is generally composed of several components: phase detector, low pass filter (LPF), voltage control oscillator (VCO), and one or more divider. The diagram for a PLL system is shown in Figure 1. Noise degrades the performance for a PLL system. It can come from within or outside the PLL. For relevant reviews on PLLs and related noise processes, we refer readers to [1][2][3] .

A PLL is described and quantified in terms of its transfer function that can be represented in either the time–domain or the frequency-domain. The frequency-domain response function, is, in general, an nth order fractional function that has zeros/poles. The PLL output is the interaction of input signal, noise processes, and transfer function. At the design stage, input signal form, noise temporal and spectral form, and the transfer function can be assumed or determined, and that simulating the output signal in both time and frequency domain is a standard forwarding problem. However, at the prototype IC stage, the situation is different and more difficult. All we can access is the input and output of the PLL. On the other hand, it is very important to measure the PLL transfer function and noise processes so that design specifications and simulation assumptions can be checked and verified and potential design flaws and noise sources can be identified, and then fixed or improved.

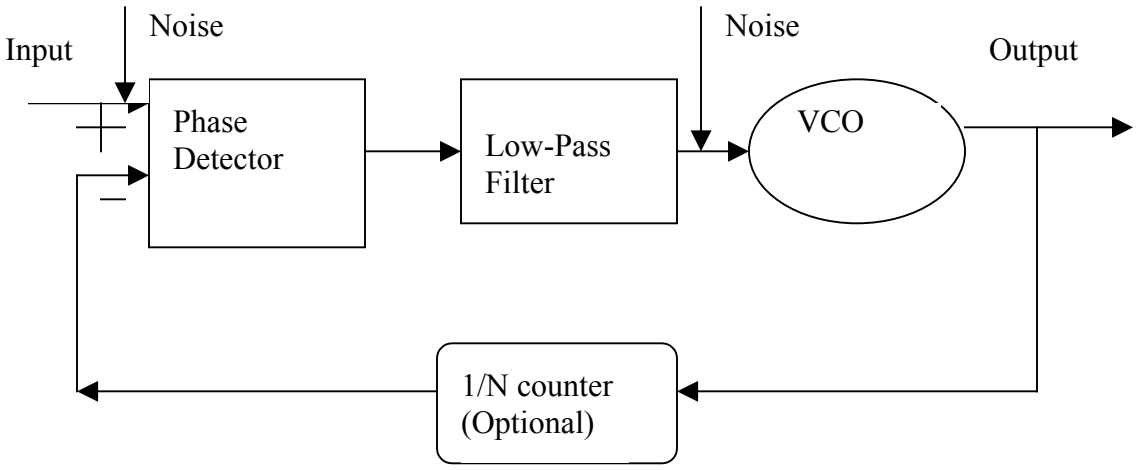

Figure 1. A PLL block diagram. The noise can be within and/or outside the loop.

In addition to clock generation with either multiplied or divided frequency output, PLLs are widely used in modern serial communication to recover the clock from data bit stream. The recovered clock must have as small noise/jitter as possible, otherwise the receiver performance will be degraded and the bit error rate (BER) of the system will increase. The performance of the PLL depends on individual components, system transfer function, noise origin and interaction processes between them.

2.) PLL Transfer Function and Noise

As we have mentioned, a PLL is essentially a complicated feedback system. Because of that, a system level modeling is needed in order to understand the physical processes. Three aspects are essential, one is the overall loop transfer function that is determined by its component characteristics; another is the noise process, their origin and spectrum shape; and the third one is the interrelationship between loop transfer function and noise process, and how it affects the overall performance of the PLL. One can address these aspects from the time domain, or the frequency-domain, or both. Each domain has its own advantages and disadvantages, and we will give a general introduction in the following sections.

2.1) Time-domain modeling and analysis

Although a PLL is traditionally studied and modeled in frequency domain, time-domain modeling can offer some unique information that the frequency domain generally could not for most of the practical applications. For example, phase information of a signal is available in time domain if it is measured by either a sampling or a digitizing oscilloscope, while it is not available in frequency domain if it is measured by a spectrum analyzer. However, on the hand, PLL time-domain system impulse response is hard to deal with mathematically, particularly if it is a second or higher-order PLL. The following is a simplified diagram in for a time-domain PLL block diagram

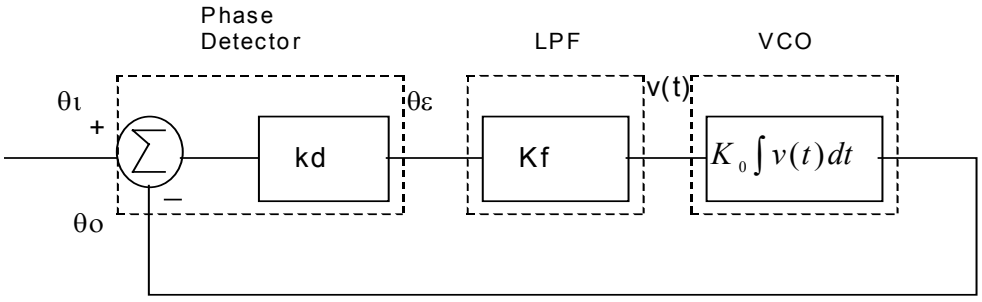

Figure 2. Time-domain modeling of a PLL

In this example, the LPF is simplified by a constant gain factor of K_f. The equation determines the phase error and input phase is given the following:

$$\theta_e(t) = K_d(\theta_i - K_0 K_f \int \theta_e dt) \tag{1}$$

An integral equation is generally hard to solve so we take the derivative of equation (1) and obtain equation (2) of the following

$$\theta_e^{'}(t) + K_d K_f K_0 \theta_e = K_d \theta_i^{'} \tag{2}$$

Once θ_e is solved, the θ_o is readily obtained by the relationship of $\theta_o = \theta_i - \theta_e$.

Equation (2) has a general solution of

$$\theta_e = e^{-Kt}(\int e^{Kt}\theta_i(t)dt + c) \tag{3}$$

Where $K = K_d K_f K_o$ is the overall loop gain. It can be seen that θ_e has an exponential decay envelope indicating that the phase error decreases as time increases. However, whether θe will decay to zero or a constant phase error depends on the input phase error. If the θ_i = constant, it can be shown that as $t \to \infty$, $\theta_e \to 0$, i.e., a PLL locks to its frequency with a zero phase error; if the phase increases with time linearly, i.e., $\theta_i = \omega t$, then it can be shown that as $t \to \infty$, $\theta_e \to$ constant, i.e., a PLL can lock to its frequency but with nonzero error.

The time-domain PLL study indicates several points: i.) when the PLL is a first order system (i.e., LPF has a constant gain), it can be modeled by a closed form solution; 2.) it is hard to model the noise process and its interrelationship with loop components in time-domain. Clearly, other approaches are needed to model and analyze PLL.

2.2) Frequency domain modeling and analysis

2.2.1) Transfer function

A PLL can also be modeled in a complex frequency-domain (i.e., S-domain or Laplace domain) with the linear system assumption. A linear system assumption is a good approximation for PLLs. In the S-domain, mathematical model for a PLL with noise added can be illustrated in Figure 3. Due to the interrelationship that an integral in the time-domain is equivalent to 1/s in the S-domain, the VCO transfer function becomes K_o/s. The LPF is therefore replaced by the general function of F(s). Since this is a linear feedback system, the overall transfer function can be obtained through multiplication and division operations of the transfer functions for individual components within the system. This greatly simplifies the mathematical difficulties. The system transfer function is given by:

$$H_o = \frac{\theta_0(s)}{\theta_i(s)} = \frac{K_d K_o F(s)}{s + K_d K_o F(s)} \tag{4}$$

and the error transfer function is:

$$H_e(s) = \frac{\theta_e(s)}{\theta_i(s)} = \frac{K_d s}{s + K_d K_o F(s)} \tag{5}$$

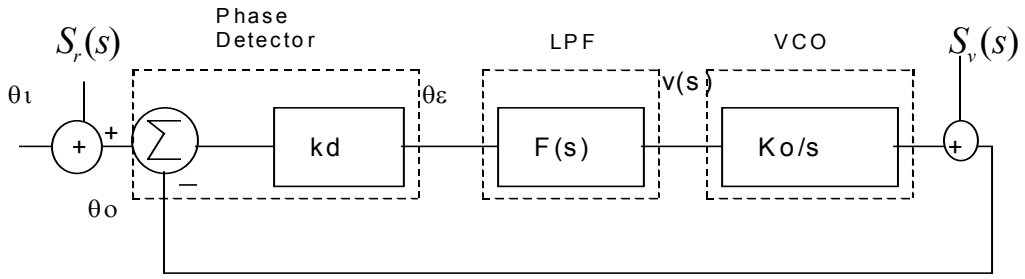

Figure 3. S-domain PLL model illustration. Note that the noise due to input signal and VCO are indicated as additive processes.

From equations (4) and (5), it can be seen that once the transfer function is given, the out signal θ_o is readily obtained for a given input signal θ_i in the S-domain. The time domain response can then be solved through the inverse Laplace transformation.

2.2.2) Noise power spectrum density (PSD)

Traditionally, A PLL noise process is quantified by the overall noise power and noise bandwidth. The major shortfall of this approach is that it does not give the dynamic aspect of the PLL behavior. The question of how does the PLL noise/jitter change as a function of time/frequency is not addressed by noise bandwidth and noise power. A more comprehensive method is needed to address the dynamic aspect of the PLL noise/jitter behavior. If we assume that the noise contributions in a PLL is additive, and if we know which component the noise is associated with, then the PLL noise PSD can be estimated as we will demonstrate.

The major contributions of PLL noise/jitter come from two sources, input (or reference) signal and VCO. Here we will limit our discussion to these two noise sources. We will take the advantage of a linear system, i.e., the PSD for the output signal is related to its input through $S_{out}(\omega) = |H(\omega)|^2 S_{in}(\omega)$. By using this rule, we have (refer to Figure 3 for noise sources):

$$S_o(\omega) = S_r(\omega)\left|\frac{K_d K_o F(j\omega)}{s + K_d K_o F(j\omega)}\right|^2 + S_v(\omega)\left|\frac{s}{s + K_d K_o F(j\omega)}\right|^2 \qquad (6)$$

Where the angular frequency $\omega = 2\pi f$, and $s = j\omega$: the implication of equation (6) can be multifold. First, it relates the PLL internal and external noise PSD with its transfer functions. We have three variables here, input PSD, transfer function, and output PSD. By knowing either two of them, the third one can be derived. Second, it allows the determination of PLL internal noise PSD and transfer function parameters if the output PSD and forms of both transfer function and internal noise PSD are known. This will be the central topic for section 4.

3.) Variance and Power Spectrum Density (PSD)

In section 2, we have discussed modeling and analysis for PLL system and noise process in both time and complex frequency domain. We illustrated the advantages and disadvantages of using each domain. It becomes obvious that noise process can be easily modeled in the complex frequency domain versus in the time-domain. However, there is an important question that we have not addressed yet, i.e., when the noise PSD at the frequency domain is obtained through equation (6), can we study this effect in the time-domain? If so, what is the method? In this section, we will address this question and illustrate the applications of using the variance and PSD interrelationship to be established.

In the absence of a deterministic noise process, the variance function describes a random noise rms value change as a function of time. It can be shown that the variance function relates to autocorrelation function through the following form:

$$\sigma_t^2(t) = 2(\sigma_0^2 - R_{tt}(\Delta t_n(t), \Delta t_0)) \qquad (7)$$

Where σ_t^2 is the variance at time t, σ_0^2 is the total variance of the underline noise process, R_{tt} is the autocorrelation function between jitter $\Delta t_n(t)$ and Δt_0. It is well known that the autocorrelation function R_{tt} relates to the PSD S(f) through Fourier transformation of

$$R_{tt}(\Delta t_n(t), \Delta t_0) = \quad \Im^{-1}(S(f)) \qquad (8)$$

Where $\Im^{-1}$ denotes the inverse Fourier transformation. Substitute equation (8) into equation (7), we obtain the equation that relates variance time series with the frequency domain PSD of the noise process

$$\sigma_t^2(t) = 2(\sigma_0^2 - \Im^{-1}(S(f))) \qquad (9)$$

Equation (9) lays a theoretical foundation to link the noise process measurable in time domain to that in frequency domain.

4.) Application of Variance and PSD Interrelationship

Equation (9) for the variance and PSD interrelationship can be used in many ways. For example, in the simulation application, one can use it to predict time domain jitter performance if the noise PSD: S(f) in the frequency domain is known or vice versa. S(f) is a function of both PLL transfer function and noise process as we have shown section 2. As a result, we can study and probe both transfer functions and noise processes for a PLL if either the variance or the PSD is given. We will focus on measurement and analysis in this paper.

4.1) PLL Measurement and Analysis

4.1.1) Review of Traditional Methods

Traditional methods used to measure PLL system and/or component functions/parameters have the following characteristics:

i.) It requires a modulation signal source
ii.) It requires the access of PLL internal structure in most cases
iii.) It is a piece-meal approach that requires many different setups to get all the PLL related parameters and functions
iv.) It does not separate the noise from the transfer function
v.) It does not provide a means to estimate the measurement accuracy
vi.) It does not provide prediction capability

Commonly used equipments are oscilloscope and spectrum analyzer. Most methods do not have the analysis/prediction capabilities. Clearly, there is ample room to improve the current PLL measurement and analysis methodologies.

4.1.2) Variance Based PLL Measurement and Analysis Method

a.) Theory

In order to take the advantage of equation (9), an instrument that can measure variance quickly with a long enough record length is needed. Oscilloscope does not meet this requirement, while a Time Interval Analyzer (TIA) can do the job. A TIA provides a comparator based timing measurement that can measure edge to edge time intervals with a very fast measurement rate up to 2 million measurements per second, facilitating an ideal apparatus for data intensive measurement and analysis applications, such as jitter and noise analysis. Many of the practical PLLs are a second order system, and any higher system can be a approximated with a second order system. We will start with a second order PLL to illustrate the method. We assume that overall noise process is approximated by a white noise. Then we will develop an analytical model for the variance time record. By using the measured variance record and variance model, the PLL loop parameters, transfer function, and noise intensity are determined, either through curve fitting or direct solution.

The second order PLL transfer function is given by :

$$H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{10}$$

Where ω_n is the natural frequency and ς is the damping factor for the PLL. With this transfer function, variance function $\sigma^2_t(t, \omega_n, \varsigma, N_n)$ is estimated and parameters are determined by using the measured variance record, through

$$| \sigma 2_{\text{t-model}} - \sigma^2_{\text{t-measured}} | < \varepsilon \tag{11}$$

Once H(s) is determined, other parameters and functions, such as natural frequency, damping factor, damping frequency, pull-in range, pull-in time, pull-out range, pull-out time, lock range, lock time and frequency, Bode plots, root locus, poles, zeros, and stability, are readily obtained[1], [2].

b.) Experiment

The setup for the PLL measurement through variance method with a TIA instrument is relatively straight forward and simple compared with other methods and equipments. Since most PLLs have an internal reference signal so that a signal generator is not required. Figure 4 illustrates the setup.

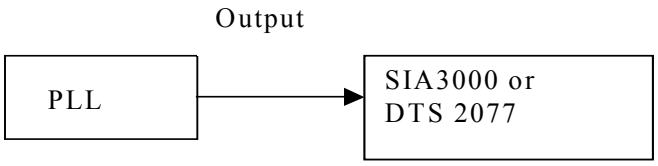

Figure 4. PLL measurement using the variance method with a TIA (SIA3000 or DTS2079) system.

The device under the test is a 50 MHz PLL clock. First, 1 sigma (squared-root of variance) data of the jitter[4] is obtained using a DTS2079 system. The equation (11) is then employed to find the best optimized parameters for the PLL. We have determined that ω_n =4.30 MHz, ς= 0.11, and $N_n = 3.16\ 10^{-7}$ μw/Hz.

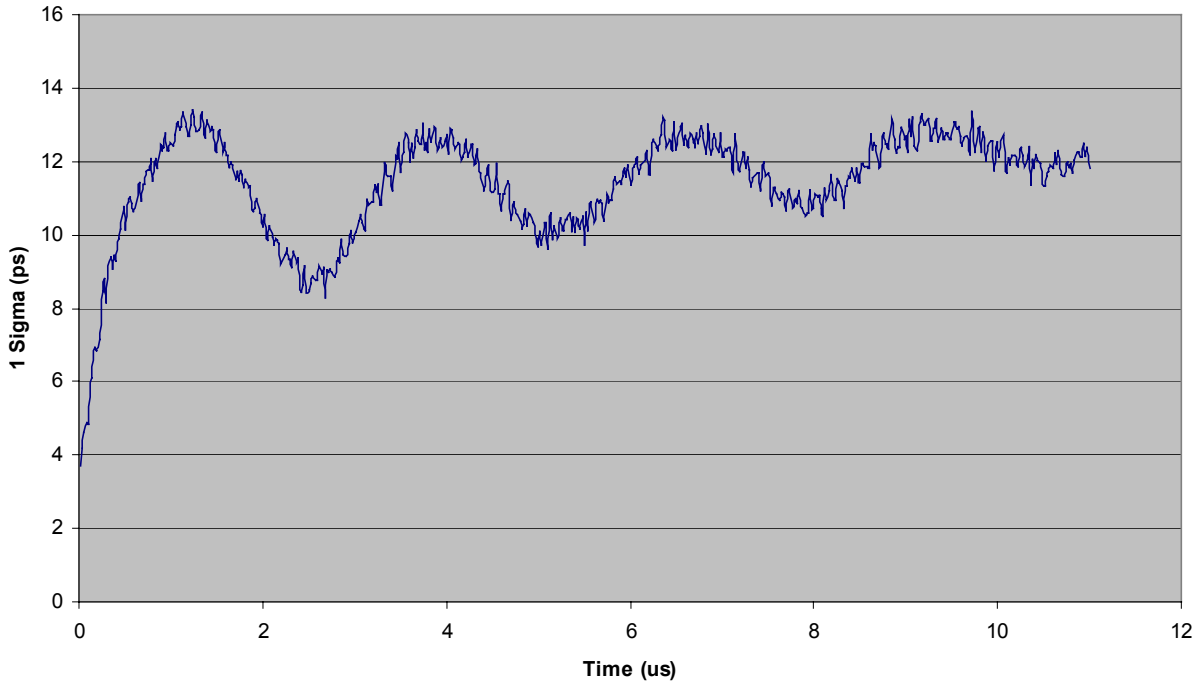

Figure 5. PLL 1 sigma time record measured by a DTS2079 system.

4.2) PLL Simulation and Analysis

Since PLL jitter and noise performance depends on loop transfer function and noise origin and characteristics, another application of our variance, transfer function, and noise PSD theory will be to simulate the PLL performance when both noise source and transfer function are given, or to optimize the PLL transfer function for a given noise source to reach a specific performance goal. The most interesting application will be in applying the new theory to simulate a PLL in conjunction with measurement. By

doing so, the loop of design-to-actual hardware verification can be closed rapidly. For example, a PLL is measured with our variance method and it is found that both natural frequency and damping factor are in error from the design specification. Then we can use the simulation tool to try different gain factors and R and C values for the LPF by considering the offset found from the first try until we achieve the desired natural frequency and damping factor in the simulation. Then we alter the hardware based the new design and simulation. This process can be repeated until we find that the PLL is compliance with specifications. This is essentially a "*in-situ*" design and verification method that bears high efficiency.

5.) Summary and Conclusion

We have developed a systematic theory that links variance, transfer function, and noise PSD for a PLL. We then apply the theory/methodology to PLL measurement and simulation. As a case study, we started with a commonly used second PLL system to show the detailed interrelationships between variance, transfer function and noise PSD. We then apply the closed form of variance that is a function of the PLL parameters of natural frequency, damping factor, and average noise power to the measured variance to determine these parameters. Other important parameters/functions, such as: locations of poles/zeros, Bode plots, root locus, lock time/range, pull-in pull-out range will be natural consequences. We also introduced applications of the variance theory/methodology to PLL simulation and analysis. We illustrated that this method bridges the gap between PLL design, debug, verification, and manufacture, and it can potentially help to short the cycle time from concept to product greatly.

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