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Jitter Transfer Functions For The Reference Clock Jitter In A Serial Link: Theory And Applications

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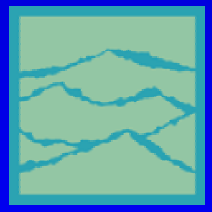

WAVECREST

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Purposes

- Understand various jitter types (phase, period, and cycle-to-cycle) and their relationships
- Determine the appropriate jitter type for digital and PLL based communication links (i.e., PCIe)
- Figure out the jitter transfer functions of reference clock and transmitter
- Suggest an appropriate and accurate jitter test methodology for reference clock and transmitter for PCIe and similar architectures

Outline

I. Review of serial data communication architectur

II. Jitter definitions

III. Jitter transfer functions

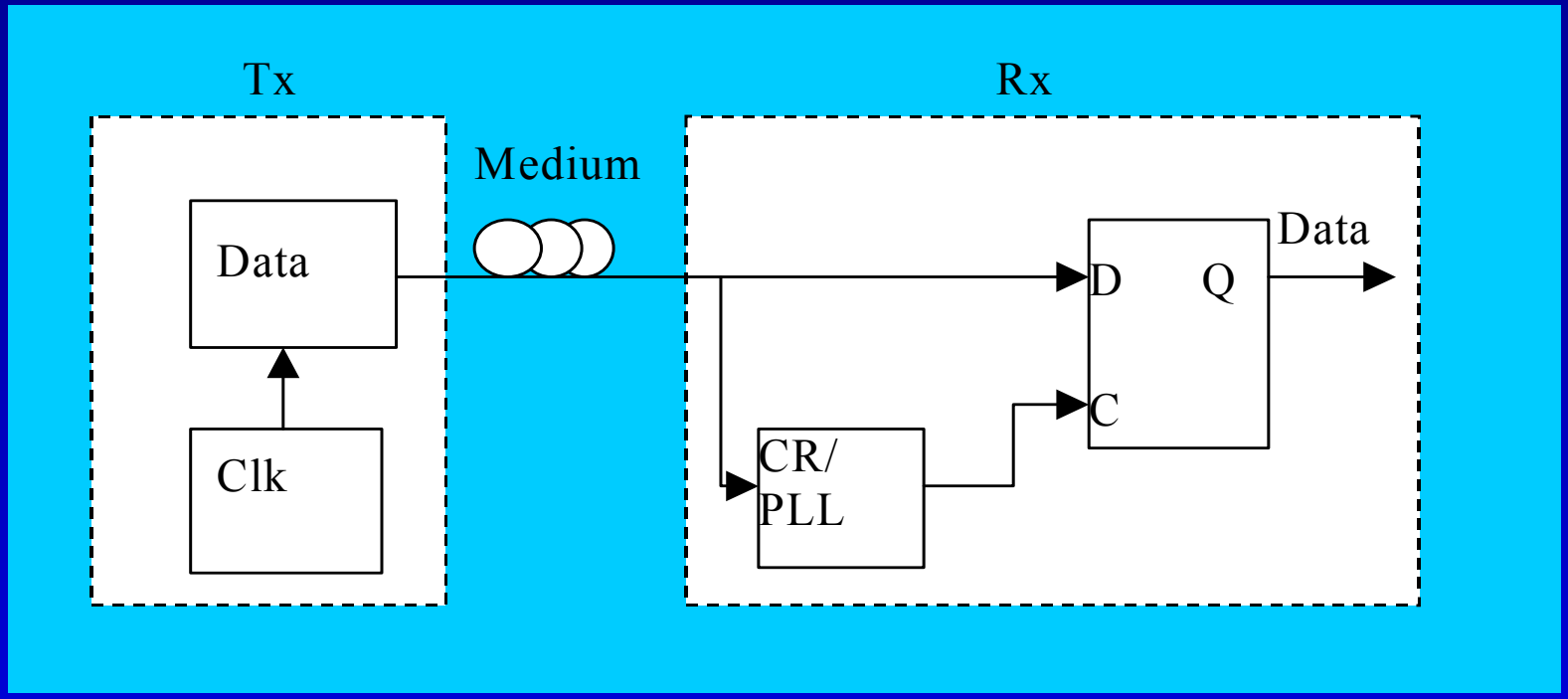
IV. System models

V. Application of the system models

VI. Summary and conclusions

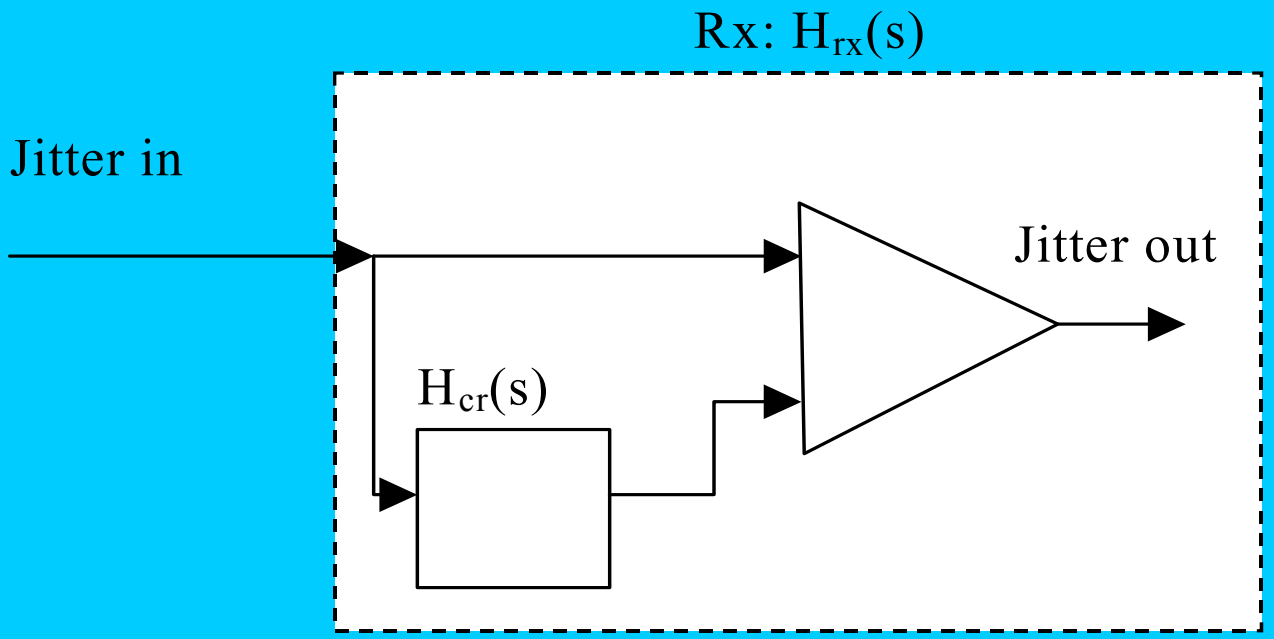
I: Overview of Data Communication

Conventional Serial Data Communication Architecture



- Bit clock is embedded in the transmitting data bits
- Bit clock is recovered via PLL at its Rx

Jitter Transfer Function In Conventional Data Communication



- "Difference function" at the sample flop
- Jitter transfer function is a ***high-pass***

II: Definitions

Units Of Jitter

- Time and Phase are used interchangeably to quantify jitter
- Difference in time is:

$$\Delta T = T_{ideal} - T_{measured}$$

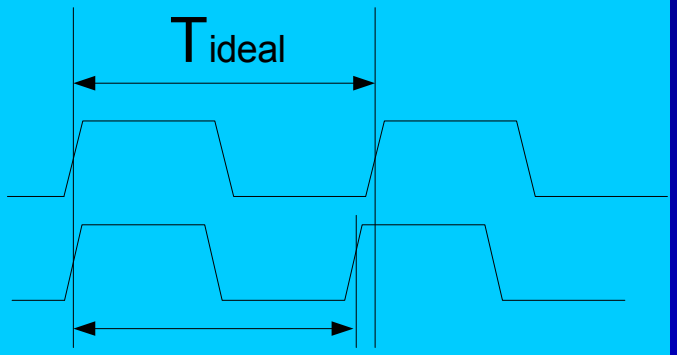
- Difference in phase is:

$$\Delta Phase = 2\pi - 2\pi \frac{T_{measured}}{T_{ideal}}$$

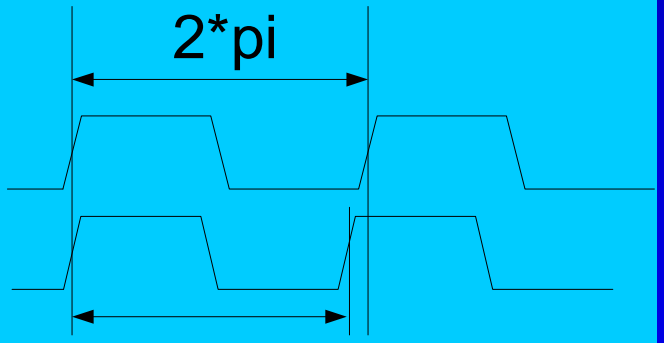
- The conversion is simply:

$$\Delta Phase = \frac{\Delta T}{T_{ideal}} * 2\pi$$

Time:



Phase:

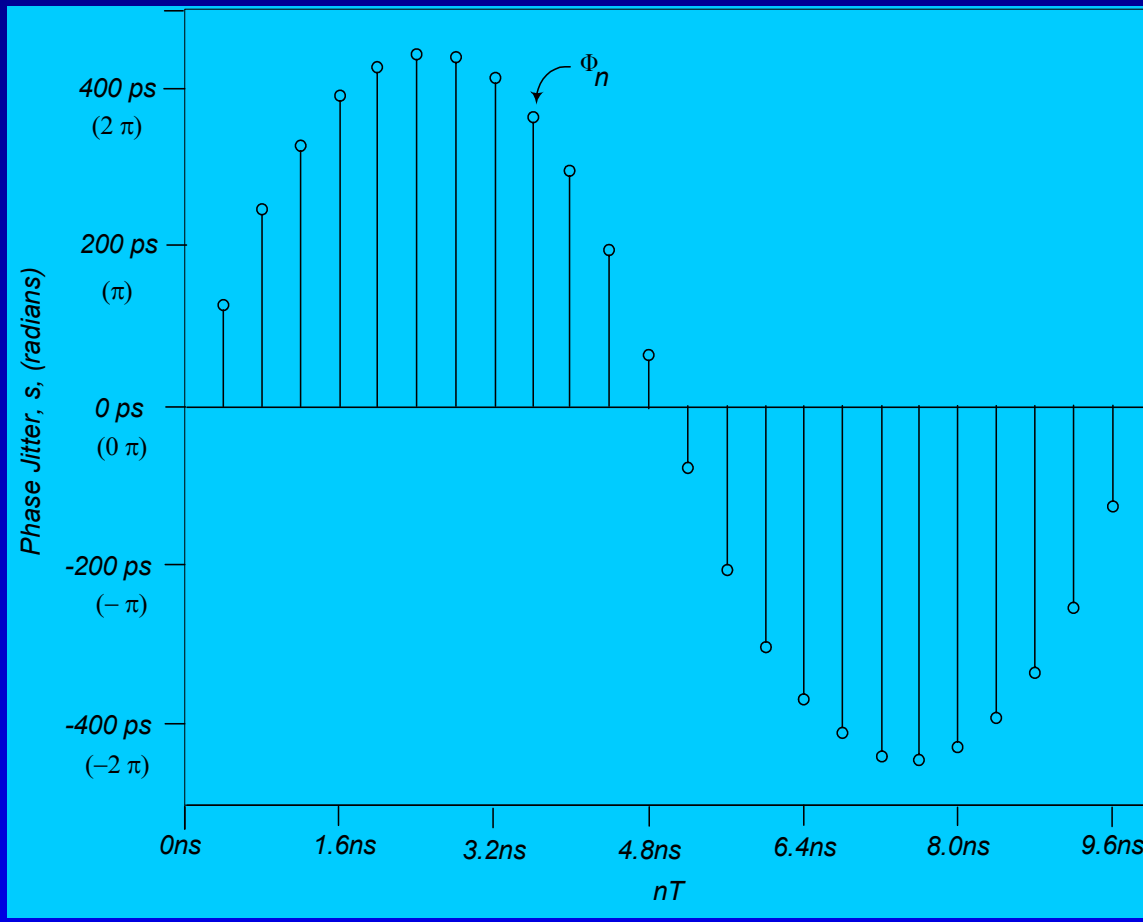


2*pi * $\frac{T_{measured}}{T_{ideal}}$

Phase Jitter (Φ)

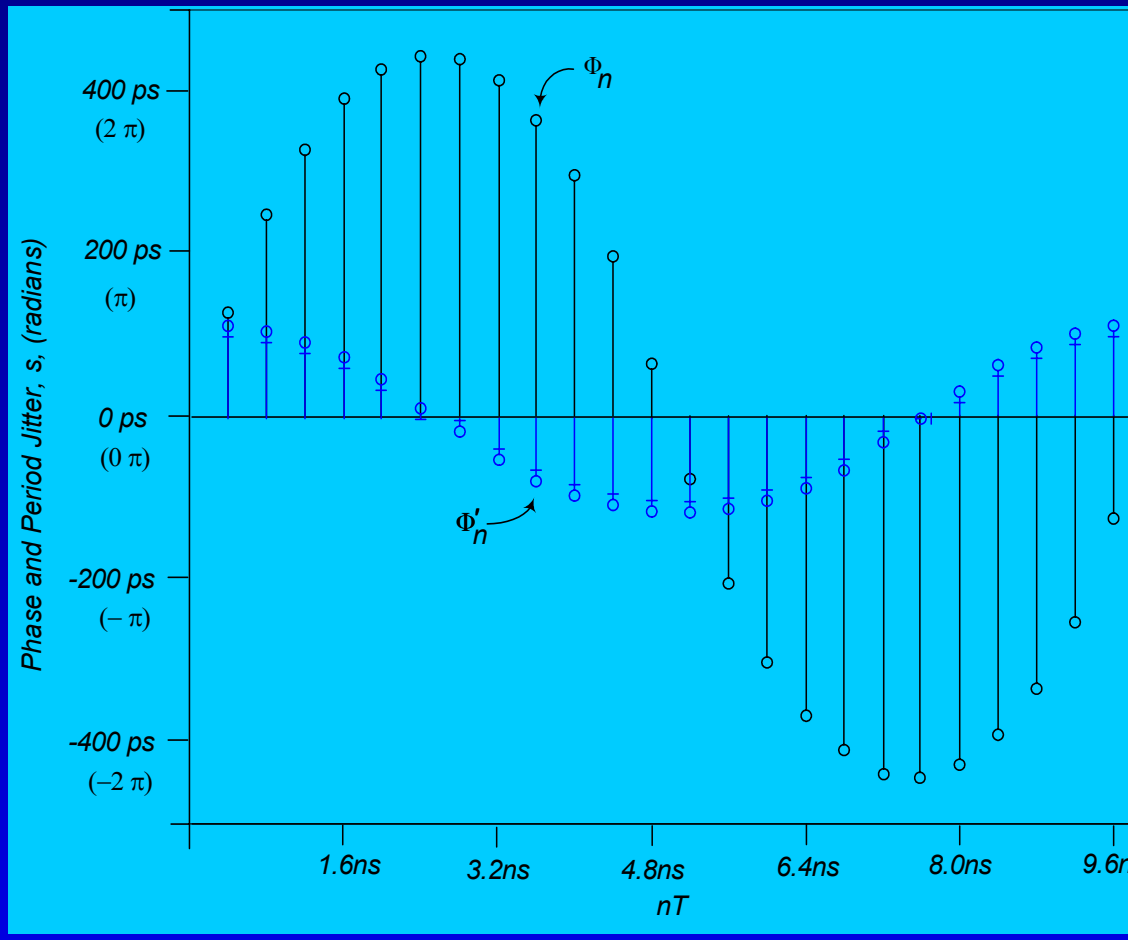
- Also known accumulated jitter

$$\Phi_n = t_n - nT, \quad n = 1, 2, \ldots, \infty$$



Period Jitter (Φ')

- Period Jitter
  - The period Jitter (Φ') is the difference between the measured period and the ideal period



$$\Phi'_n = (t_n - t_{n-1}) - T, \quad n = 1, 2, \ldots, N$$

- Also is:

$$\Phi'_n = \Phi_n - \Phi_{n-1}$$

Cycle-to-Cycle Jitter (Φ')

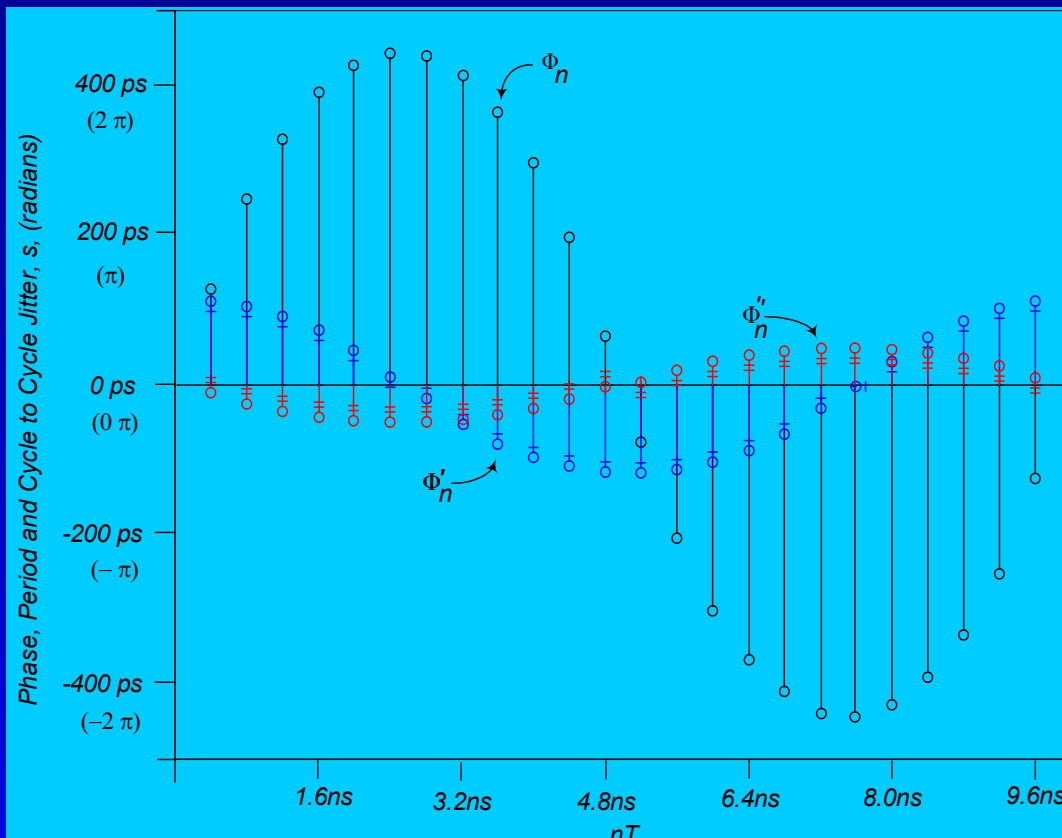
Cycle to cycle

- The difference between consecutive bit periods

$$\Phi''_n = (t_n - t_{n-1}) - (t_{n-1} - t_{n-2}), \quad n = 1, 2, \ldots, N$$

Also is:

$$\Phi''_n = \Phi'_n - \Phi'_{n-1}, \quad n = 1, 2, \ldots, N$$



Interrelationship in Time-Domain

- Phase Jitter → Period Jitter → Cycle-to-cycle

$$\Phi_n'' = (\Phi_n')' = (\Phi_n)''$$

- Cycle-to-cycle → Period Jitter → Phase Jitter

$$\Phi_n = \int \Phi_n' = \iint \Phi_n''$$

- Different representations of a same physical phenomena

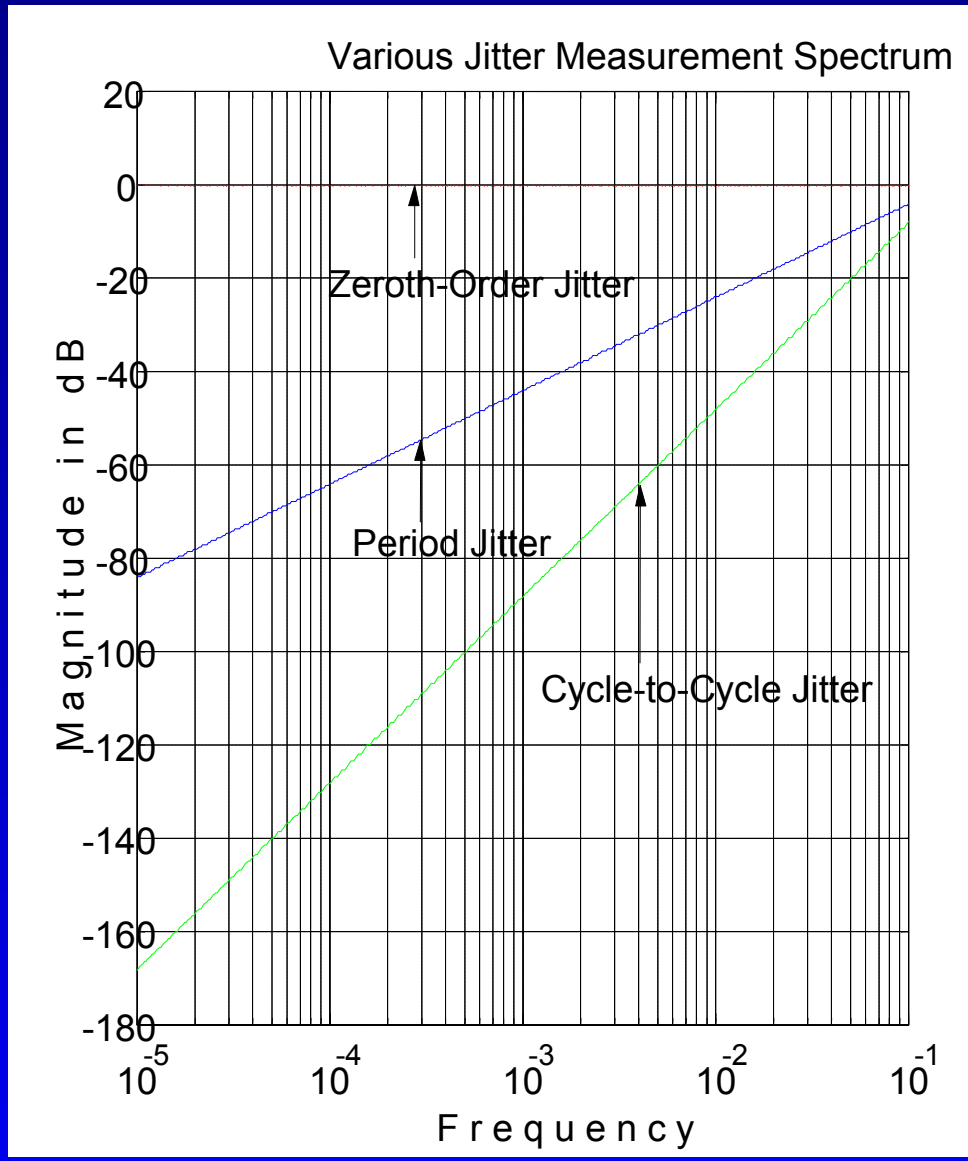
Interrelationship in Frequency-Domain

$$If\ (\Phi_{phase}(f) = c)$$

$$Then$$

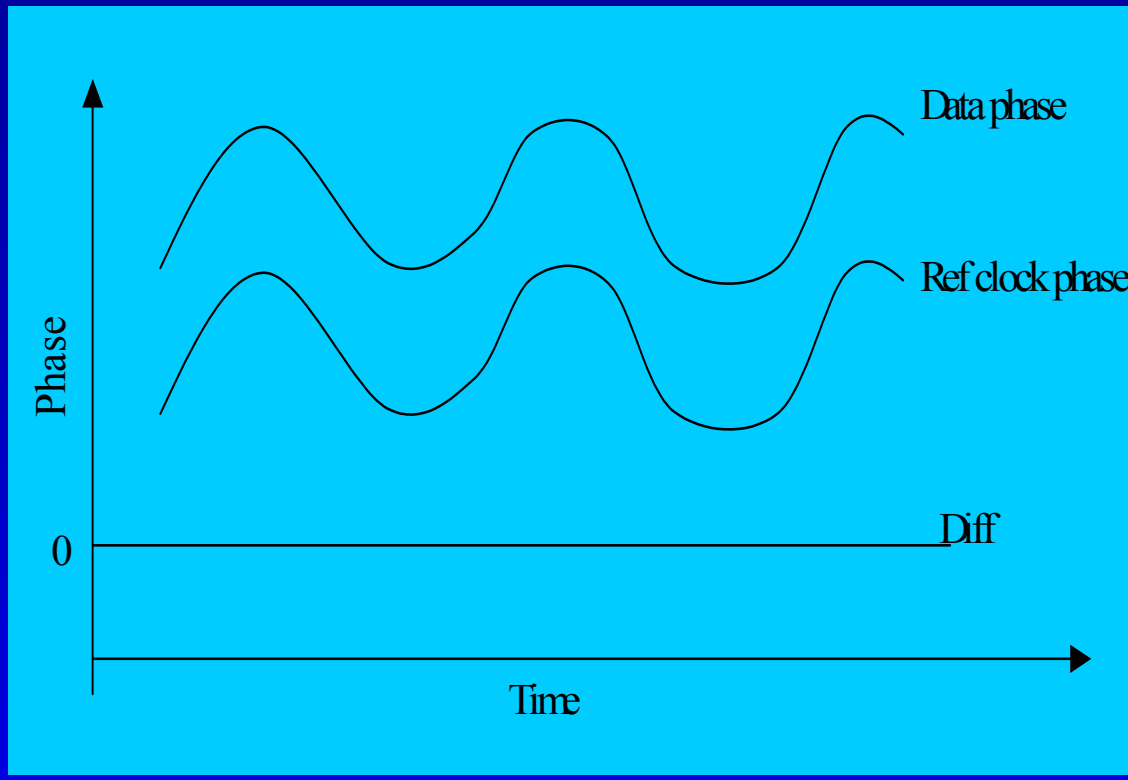
$$\Phi_{period}(f) \propto f \bullet c$$

$$\Phi_{cycle-cycle}(f) \propto f^2 \bullet c$$



Phase Jitter Measurement and Reference Clock Used

- Calculating phase jitter against a warped clock (or recovered clock) reduces the amount of phase jitter calculated
- The amount of warping depends on the recovered clock's transfer function of the receiver



Eye Closure/Total Jitter Modeling

- Given a clock and data signal

$$V_{Clk}(t) = V_{0Clk}[\omega_{Clk}t + P_{Clk}(t)]$$

$$V_{Data}(t) = V_{0Data}[\omega_{Data}t + P_{Data}(t)]$$

- Eye closure $\Delta P(t)$ is the difference in the phase between the clock and the data given by

$$\Delta P(t) = |P_{clk}(t) - P_{data}(t)|$$

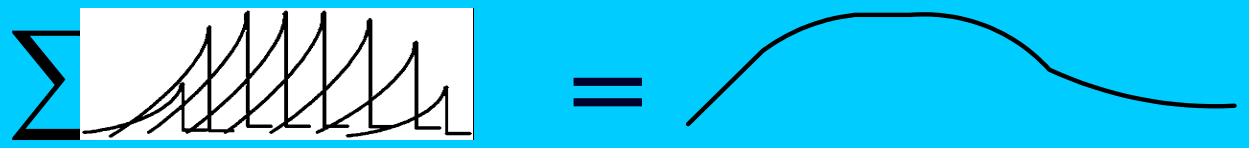
- ***Eye closure direct depends on the jitter transfer function of the receiver***

III. Jitter Transfer Functions

LTI System in Time-Domain

- An output signal y(t) equals to the input signal convolves with the impulse response h(t)

$$y(t) = \int_{-\infty}^{\infty} x(\tau)h(t-\tau)d\tau$$



- Phase jitter is modeled as continuous signal

LTI System in S-Domain

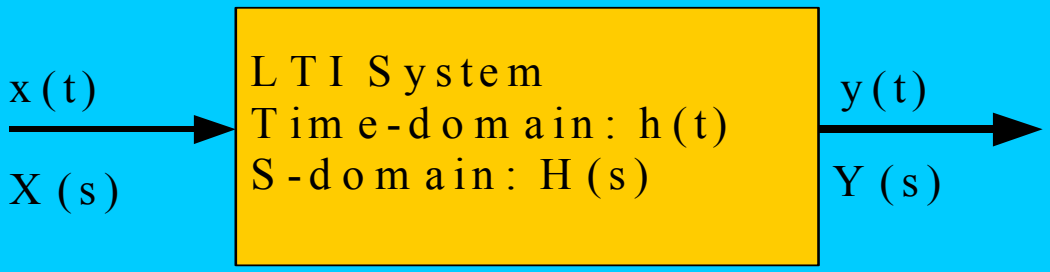
- S-domain functions is obtained via Laplace transformation

$$Y(s) = X(s)H(s)$$

$$y(t) = \text{Laplace}^{-1}\,(Y(s))$$

- Complex frequency **s** can be related to the real frequency ω through $\mathbf{s = j\omega}$, as done in the models

LTI System Summary



$$y(t) = h(t) * x(t) = \int_{-\infty}^{\infty} x(\tau)h(t-\tau)d\tau$$

$$Y(s) = H(s)X(s)$$

$$H(s) = \int_{-\infty}^{\infty} h(t)e^{-st}dt$$

IV. System Models

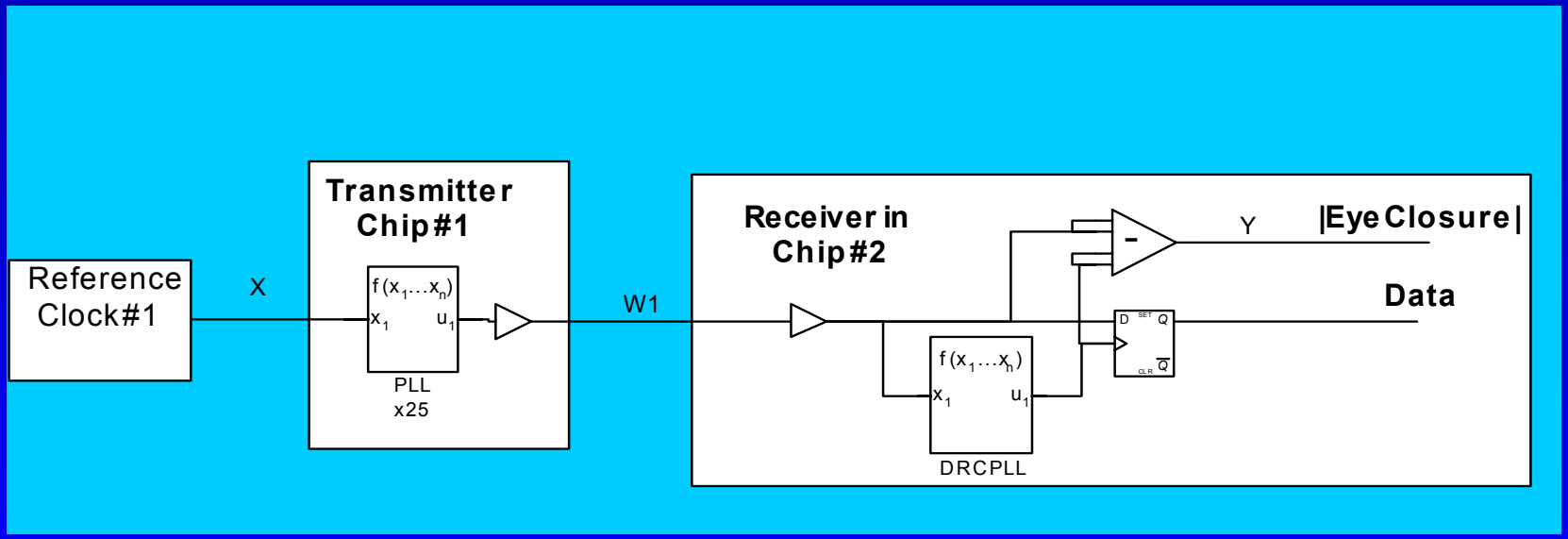
Data Recovery Circuits (DRC)

- Receiver Data Recovery is the essence of the system
- Traditional Serial Communication uses a PLL based Data Recovery
- PCI Express allows a less expensive digital based Data Recovery Circuit
  - Using phase interpolator (PI), oversampled design or digital controlled delay line
  - Majority implemented DRCs are PIs

PLL Based DRC

- The system reference clock is ***not*** used when recovering the data
- The Rx PLL needs to track the transmitter's jitter output

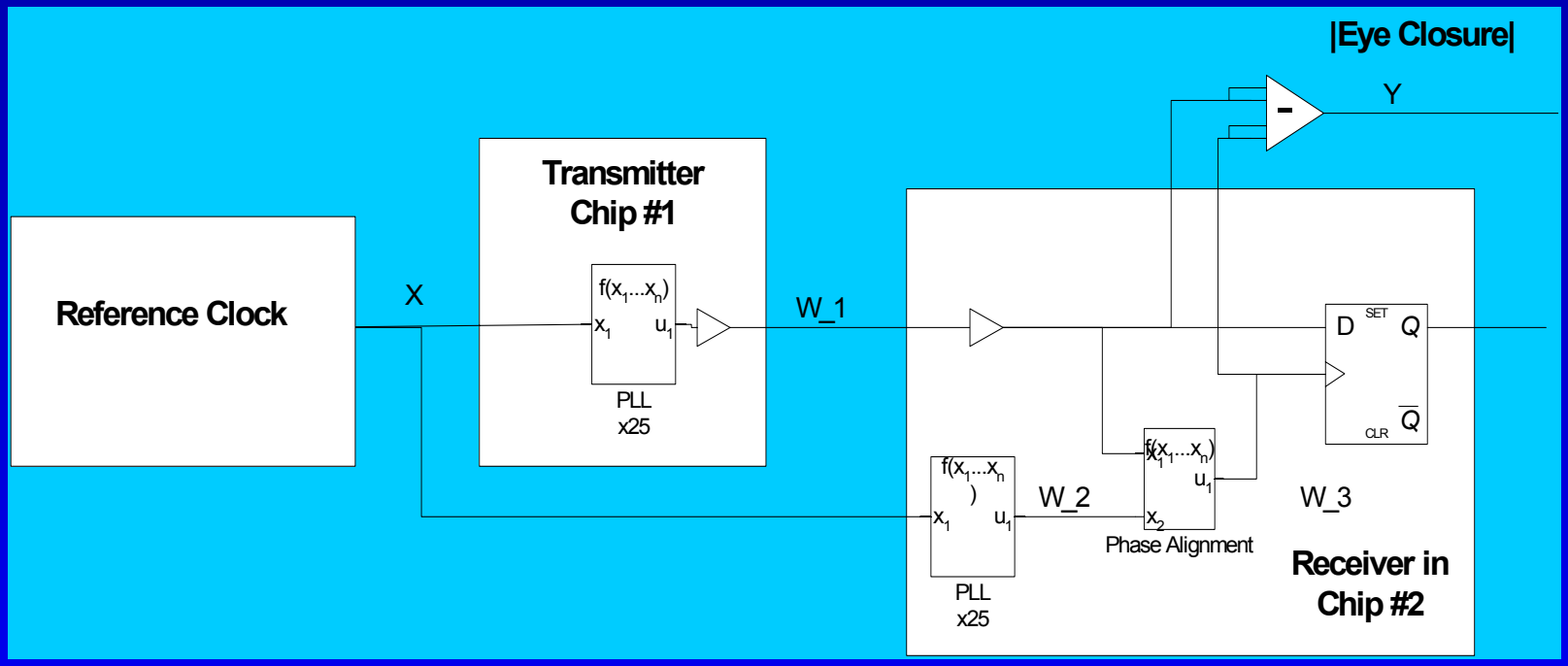
Eye-closure/total jitter system model



Digital PI Based DRC

- Both Tx and Rx use the reference clock
- Phase relationship between ref clock and data path matters

Eye-closure/total jitter system model



Phase/Jitter Transfer Function For A PLL

- The input signal to a PLL is

$$V_{in}(t) = A_{in}\sin\left(\omega_{in}t + P_{in}(t)\right)$$

where $P_{in}(t)$ is the input phase signal and is the state variable of the PLL

- The output from a PLL is

$$V_{out}(t) = A_{out}\sin\left(\omega_{out}t + P_{out}(t)\right)$$

where $P_{out}(t)$ is the output phase.

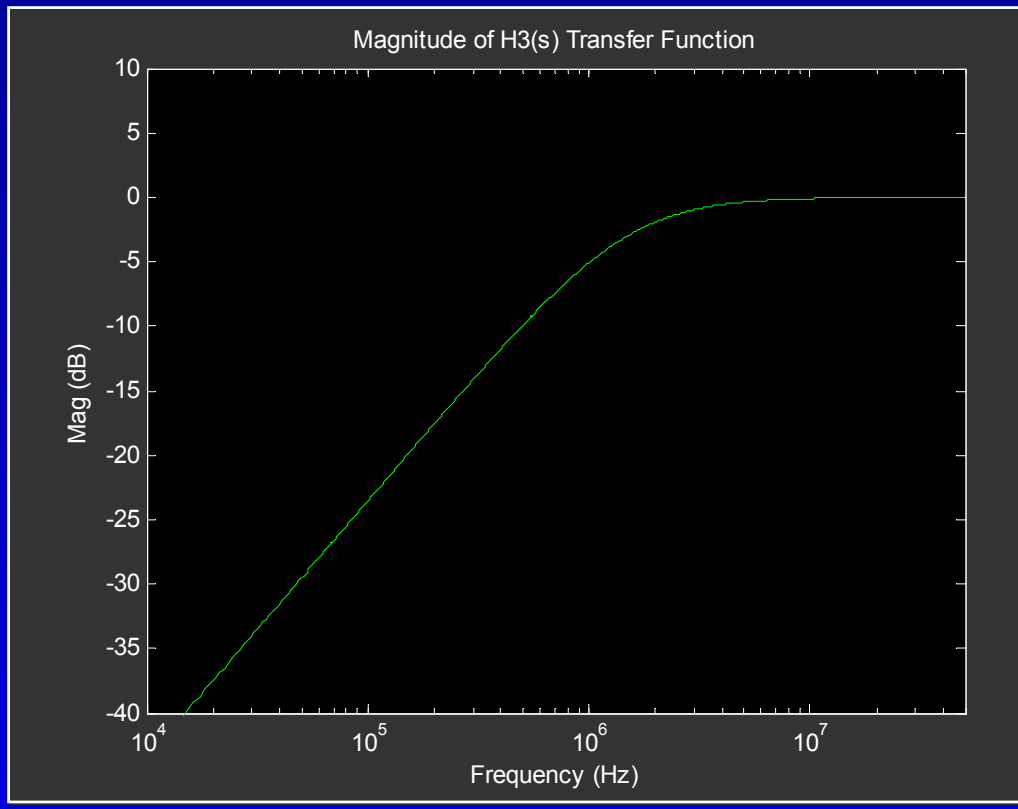
- The PLL has a phase transfer response h(t)/H(s), they satisfy

$$P_{out}(t) = h(t) * P_{in}(t) \qquad P_{out}(s) = H(s)P_{in}(s)$$

Approximate Digital PI DRC Transfer Function

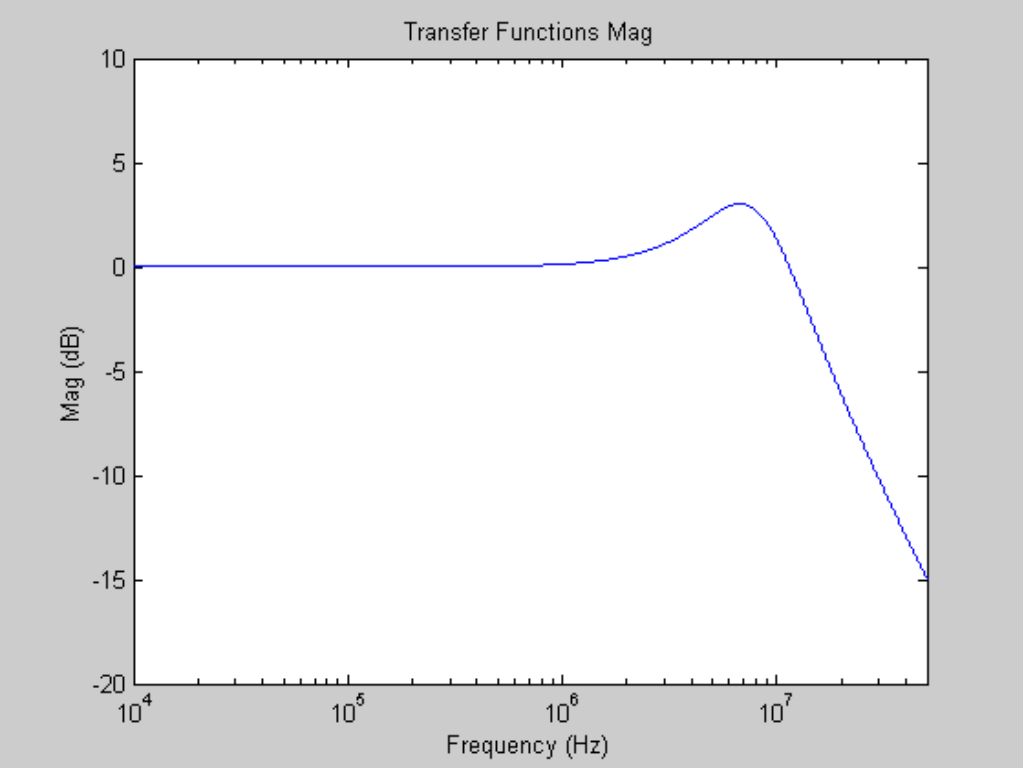
- The DRC Response is modeled by a first order F_3dB high pass = 1.5 MHz
  - This tracks the spread spectrum clock

$$H_3(s) = \frac{s}{s + \omega_3}$$



Model For A PLL Transfer Function

- Can be approximated by a 2nd order transfer functions for Rx and Tx
- Some PLLs are 3rd order or higher, additional poles at higher frequency do not contribute significantly to the eye closure

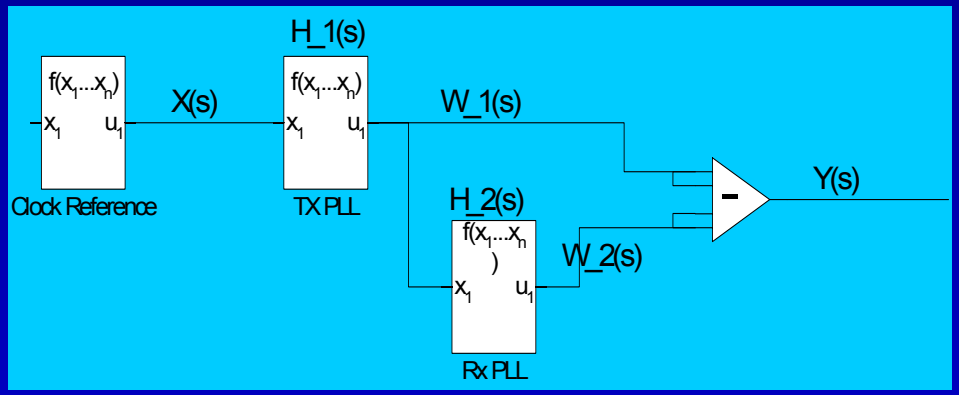


$$H1(s) = \frac{2s\zeta\omega_n + \omega_n^2}{s^2 + 2s\zeta\omega_n + \omega_n^2}$$

$$\omega_{3dB} = \omega_n \sqrt{1 + 2\zeta^2 + \sqrt{(1 + 2\zeta^2)^2 + 1}}$$

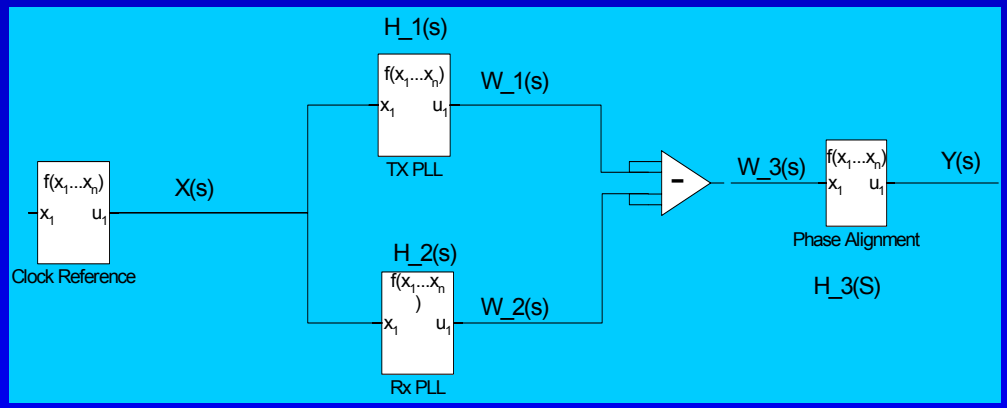
System Transfer Function Models

PLL Based DRC Model



$$H_t(s) = H_1(s)\left(1 - H_2(s)\right)$$

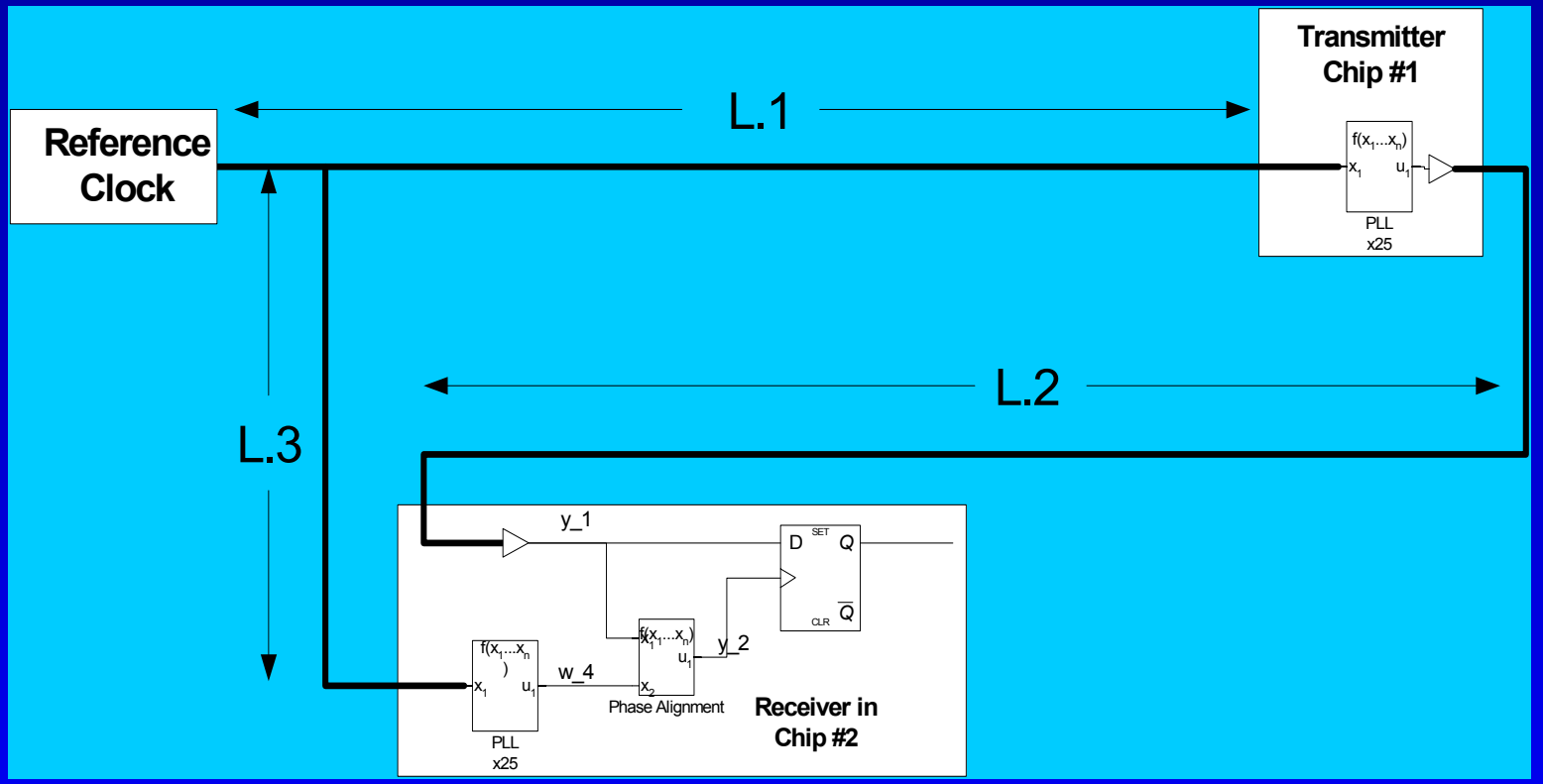
Digital PI DRC Model



$$H_t(s) = (H_1(s) - H_2(s))H_3(s)$$

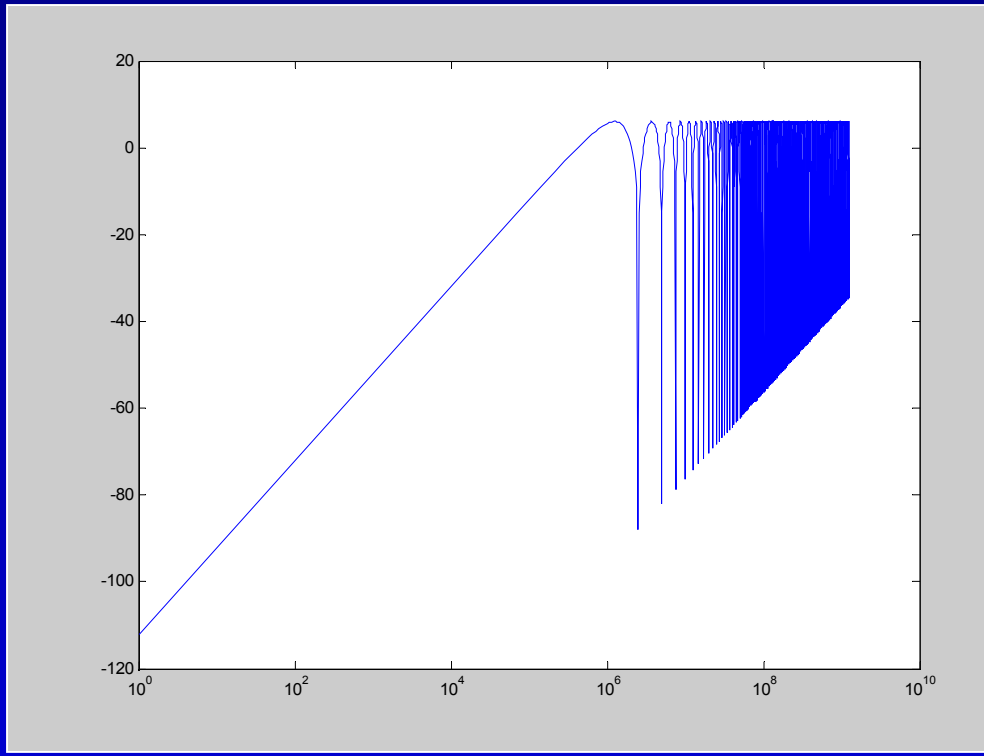
Delay Model

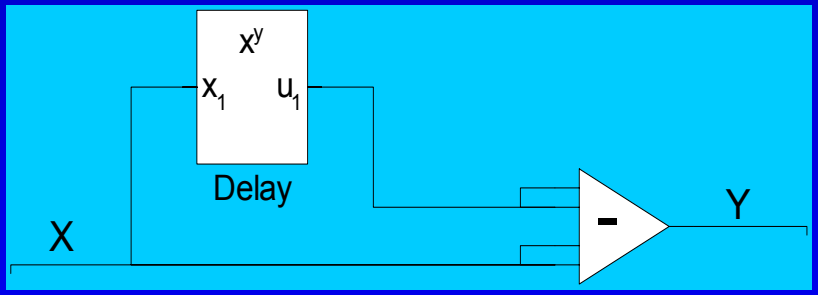
- Delay transfer function models into the system
  - The phase delay is given by (L1 + L2) – L3
  - This is modeled by exp(-s * t_delay)



Delay Transfer Function

- Example with 100 ns Delay
- The transfer function has nulls at the delay period
- It has 6dB of gain at ½ intervals of the delay period
  - Doubles the effective jitter

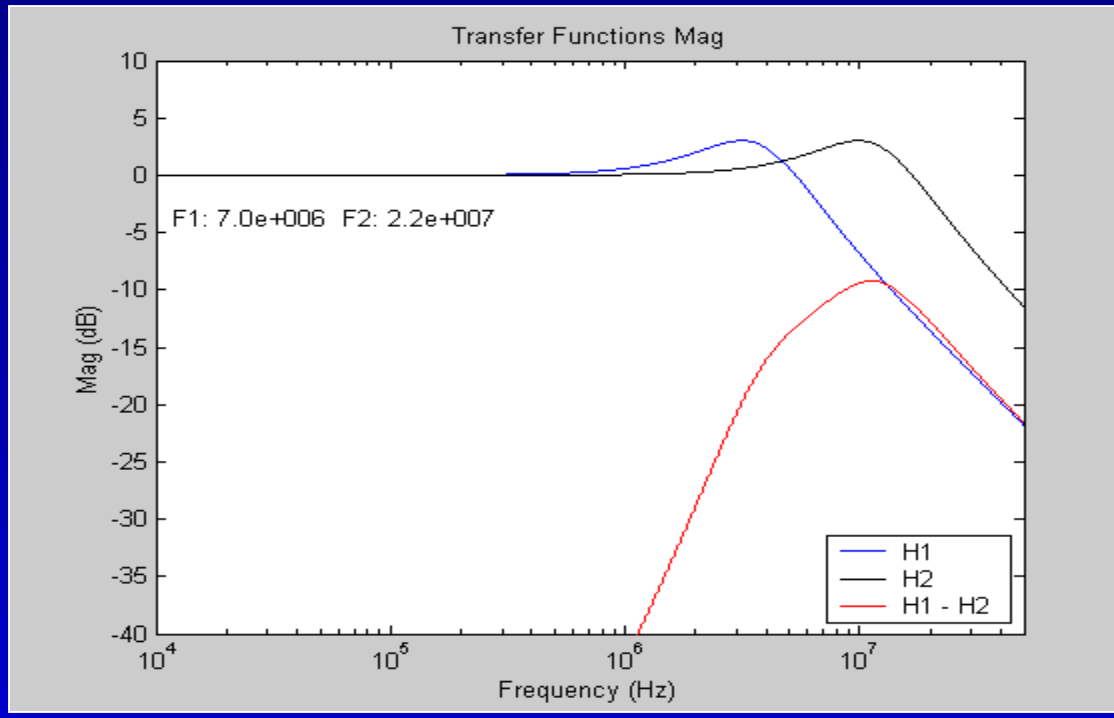


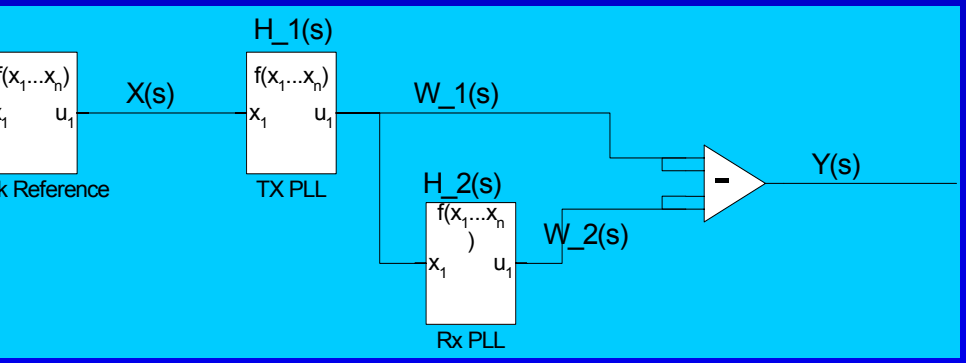


$$Y = X[1 - \exp(s * t\_delay)]$$

PLL Based Transfer Function

- PLL Based DRC does not have delay dependencies
- PLL locks to the data rate and wants a high Rx PLL response for best performance





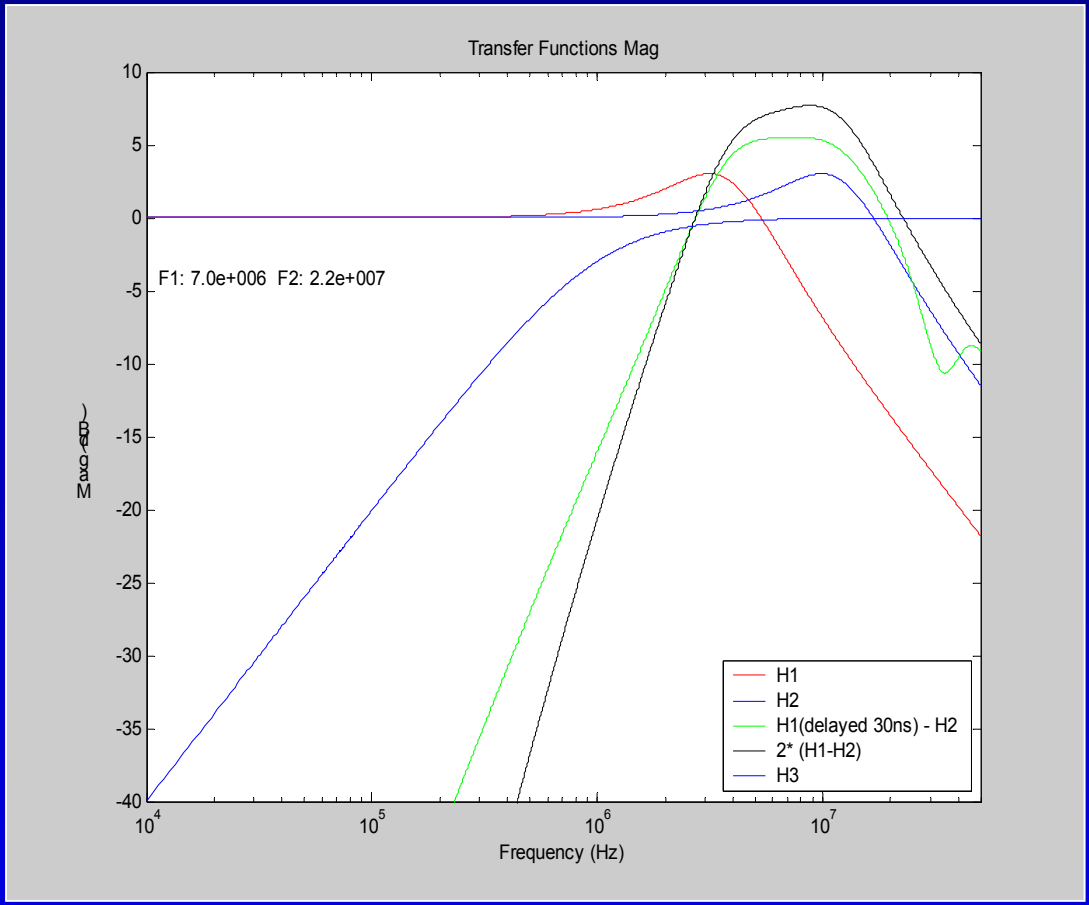
$$H_t(s) = H_1(s)\left(1 - H_2(s)\right)$$

Digital PI Based Transfer Function

The difference function includes an arbitrary phase delay not to exceed 30 ns

- The delay "un-correlates" the clock/data and closes the eye

This can be estimated with 2X multiplier of H1(s)-H2(s)



$$H_t(s) = 2\,[H_1(s) - H_2(s)]H_3(s)$$

V. Applications of System Models

Reference Clock Jitter Induced Eye-Closure Estimation

- Quantify system-level interdependencies
  - Reference Clocks
  - PLL parameters
- Calculate eye closure from the reference clock (most complex transfer function)
  - Using previously defined models

PLL and Digital PI Parameter Ranges

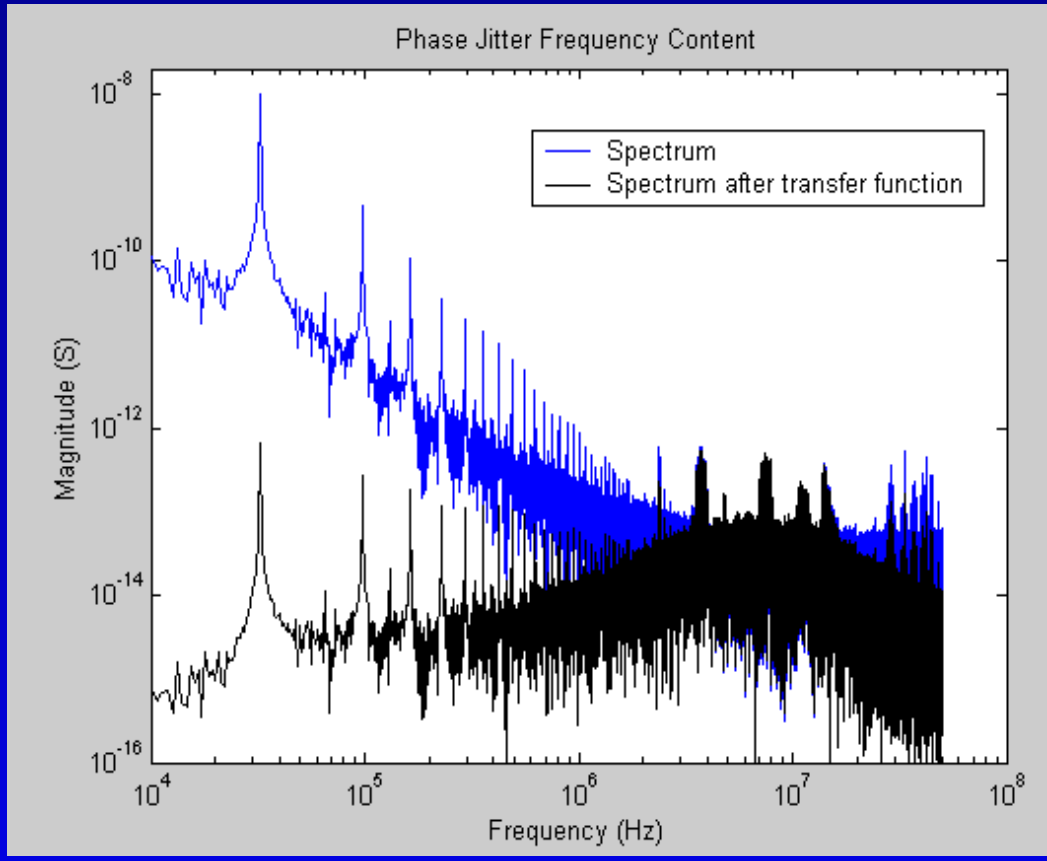
1. The BW of the Tx and RX PLLs is 1.5 MHz to 22 MHz, 3dB peaking maximum

2. The BW of the DRC (PI) should be at least 1.5 MHz

Models Applied to Measured Data: One Method

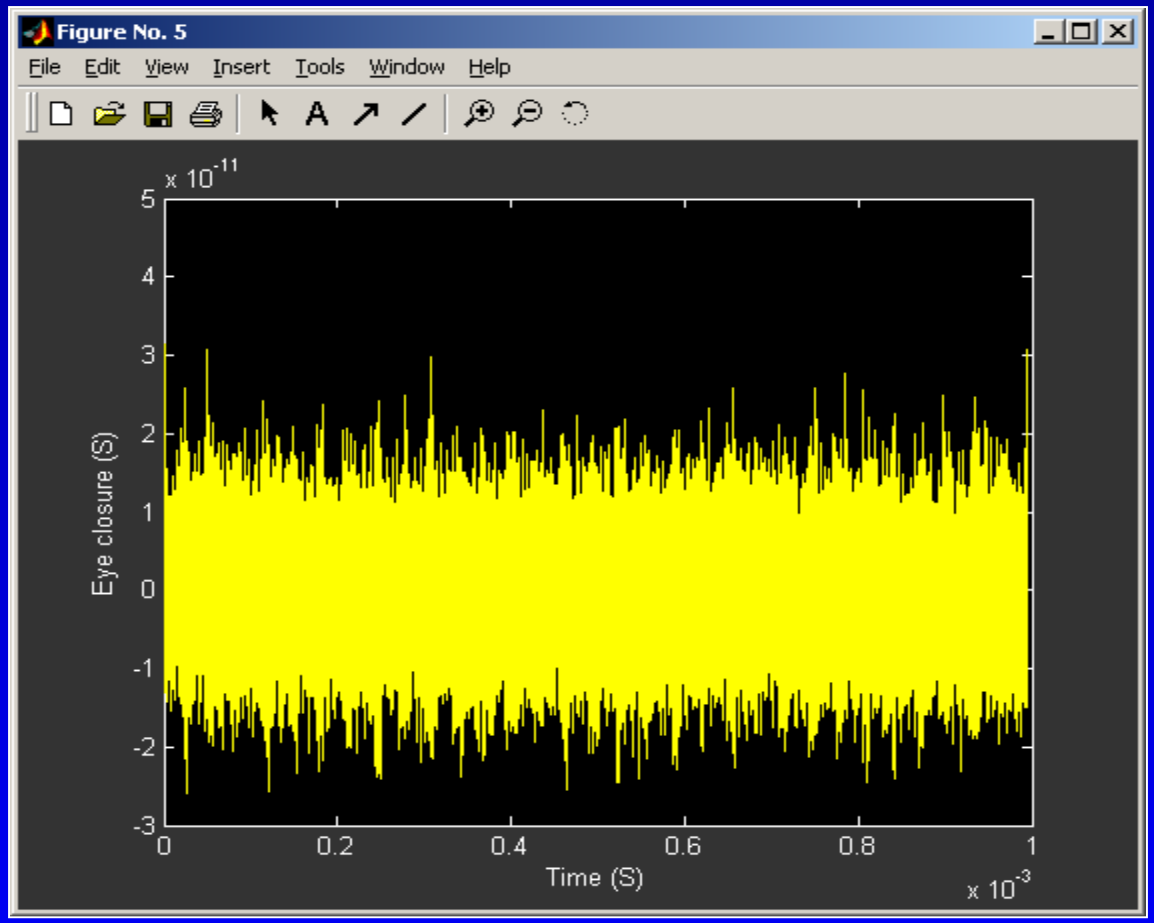
- X(s)
  - The input spectrum can be measured by measuring a clock and applying the jitter definitions to get the phase jitter
  - The phase jitter signal is then transformed into the phase jitter spectrum, X(s)
- H(s)
  - The models presented here give Ht(s), the bounding function, including the delay
- Y(s)

  Y(s) =X(s)H(s)



Eye-Closure at The RX Sample Flop-On Method

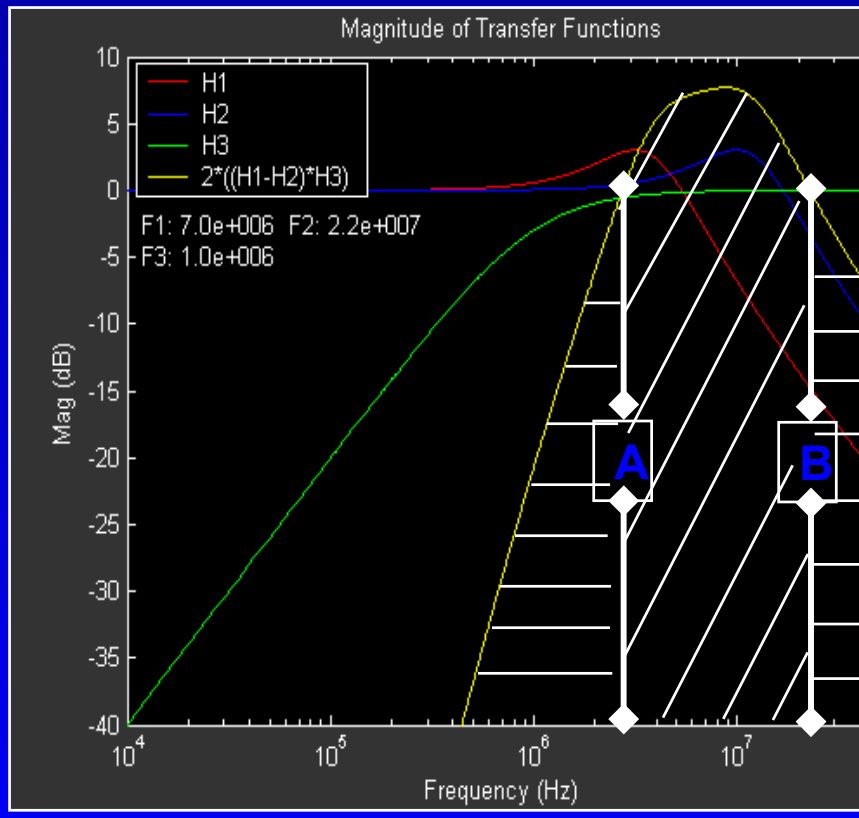
- The inverse Laplace transform of Y(s) gives the eye closure in the time domain, y(t)



Jitter "Peaking" and Broadening

- Difference function dominated by Tx, Rx and Phase Interpolator
  - PLL bandwidth difference
  - PLL peaking
- Reference clock noise spectrum as seen at Tx and Rx
- Any noise under the difference function can cause phase jitter

- 3 Danger Areas (7-22 MHz shown)
  - Between "A" and "B" ref clock jitter gets multiplied
  - Left of "A" rolls off
  - Right of "B" rolls off
- Changing Tx, Rx below 7 MHz increases width of danger areas
  - Width and Amplitude
  - Impact varies with clock spectrum



VI. Summary and Conclusion

- A quantitative mathematical ***relationship*** between ***phase, period, and cycle-to-cycle jitter*** is develope
- A ***generic*** S-domain ***jitter transfer functions*** for PCIe were established
- The jitter state variable is ***Phase Jitter,*** and ***cycle-to-cycle is not*** the right merit for PCIe clock jitter
- Reference clock jitter transfer function is a ~(3th high-2th order low) ***band-pass***
- Tx jitter transfer function is a ***1st order high-pass*** with a 3dB frequency of ***1.5 MHz***
- The method developed here ***can also be applied*** to ***new and relevant*** communication architectures (i.e., FB DIMM, SATAII etc.)