ITC 2003

A Generic Test Path and DUT Model for DataCom ATE

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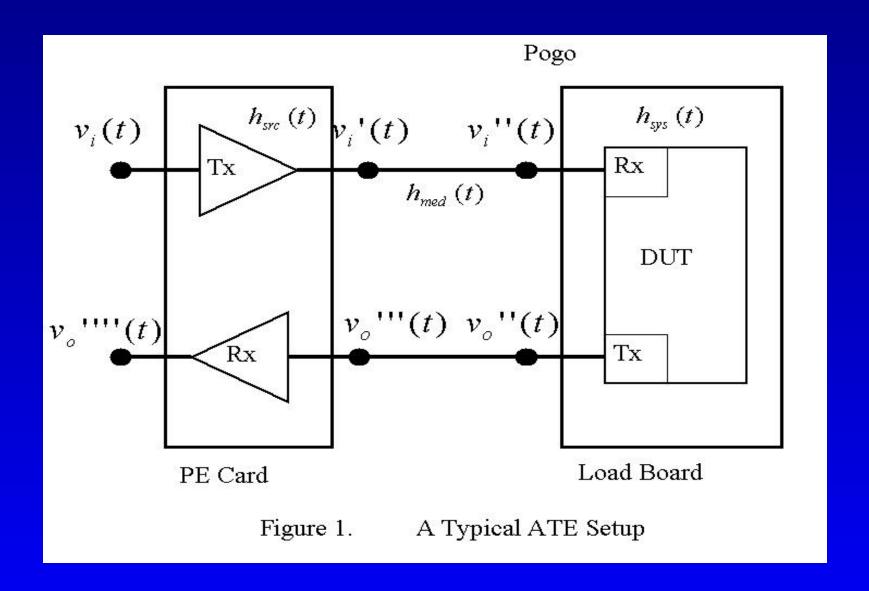
Purposes

- Understand how will a transfer function impact the deterministic jitter (DJ) in a linear system
- Introduce a generic model for quantifying DJ for an I/O path
- Apply the linear system/generic model method to analyze a high-speed ATE path

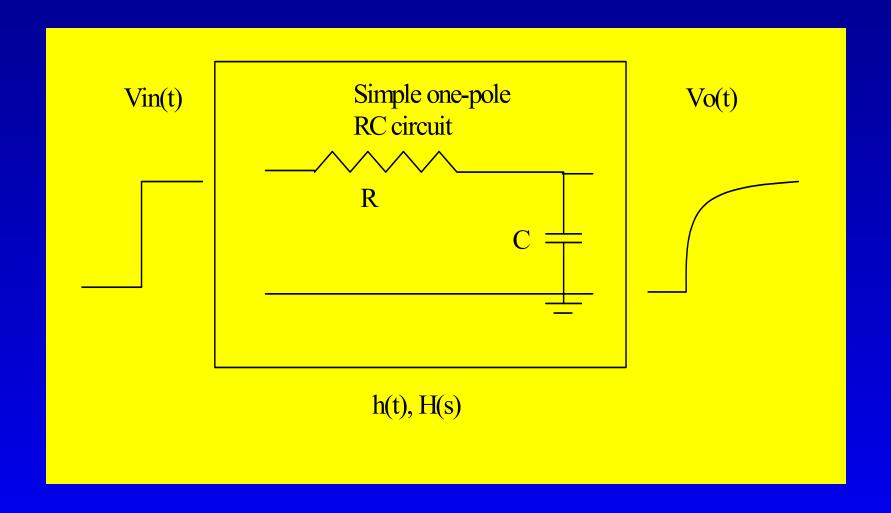
Outline

- Overview of an ATE high-speed I/O path
- Review of existing analysis methods
- Introducing a generic, pole/zero based model/analysis method
- Simulation results of the new method
- Application of the generic method to ATE high-speed I/O path analysis
- Conclusion

ATE High-Speed I/O Path



Review of A Simple One-Pole System



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Limitations of The One-Pole Model

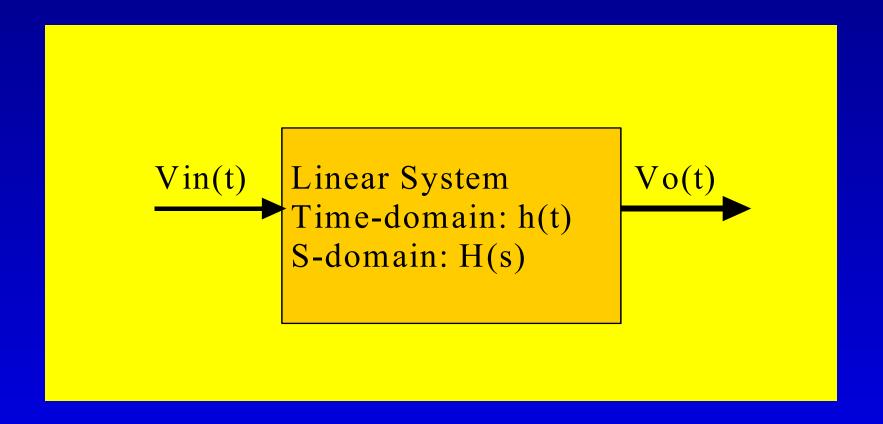
- Cannot handle dynamical aspects of the step response (I.e., ringing, damping, overshoot, undershoot etc.)
- Does not emulate most of the high-speed I/O paths
- Amplitude ISI effect is shielded

What is Needed?: A Generic, N-pole, M-Zero Model

Goals:

- Eliminate those limitations for the one-pole 1st-order model
- Scalable and generic
- Comprehensive and accurate

Review of Linear System Theory:



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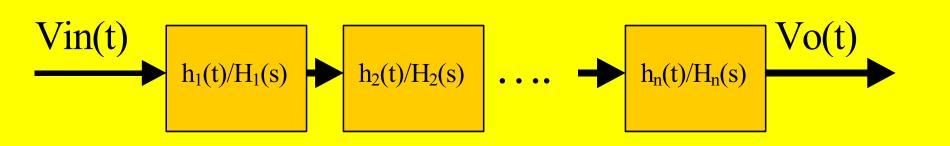
Review of Linear System Theory Cont:

$$H(s) = \int_{-\infty}^{\infty} h(t)e^{-st} dt$$

$$V_0(t) = h(t) * V_i(t) = \int_{-\infty}^{\infty} h(\tau) V_i(t - \tau) d\tau$$

$$V_0(s) = H(s)V_i(s)$$

ndependent and Cascade Linear System



$$h(t) = h_1(t) * h_2(t) * \dots * h_n(t)$$

$$H(s) = H_1(s) \bullet H_2(s) \bullet \dots \bullet H_n(s)$$

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A Generic N-Pole, M-Zero Model

$$H(s) = K \frac{s^{M} + a_{M-1}s^{M-1} + \otimes + a_{0}}{s^{N} + b_{N-1}s^{N-1} + \otimes + b_{0}}$$

$$= K \frac{\prod_{m=1}^{M} (s + z_{m})}{\prod_{n=1}^{N} (s - p_{n})}$$

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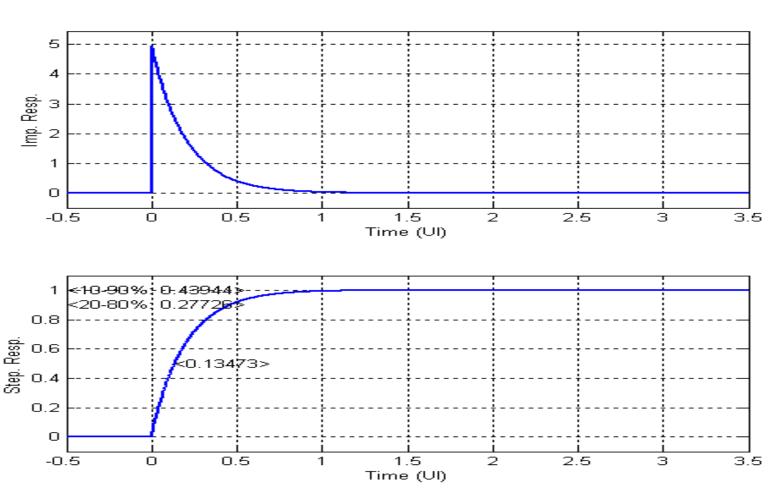
Requirements for A Generic Model

 It must be stable, i.e., all the poles are located on the left half of the S-plane, and the number of poles is >= the number of zeros

 It must be causal, i.e., the region of convergence (ROC) is right to the rightmost pole

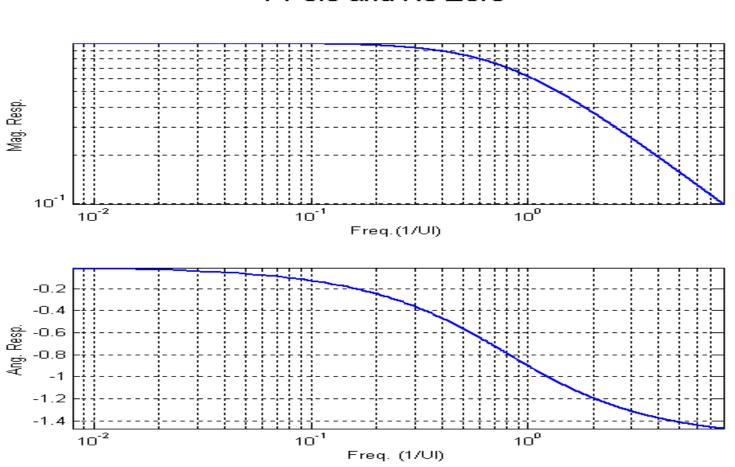
Case Study I: 1-Pole, 0-Zero (Time-domain)

1 Pole and No Zero



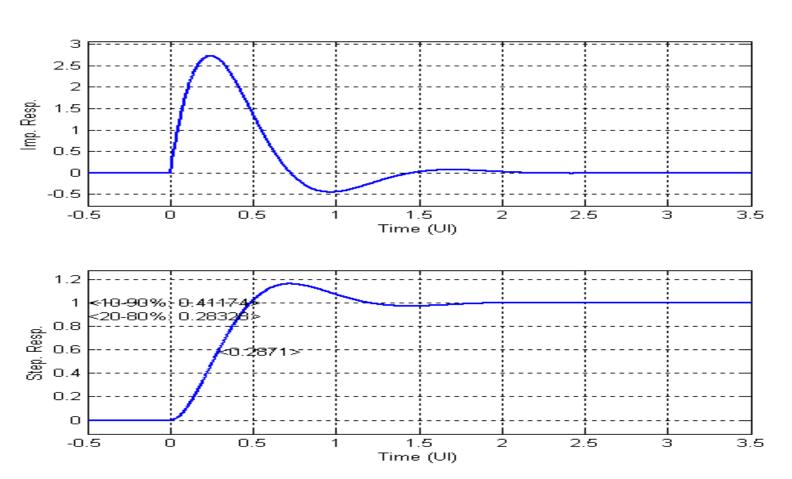
Case Study I: 1-Pole, 0-Zero Cont.. (Frequency-domain)



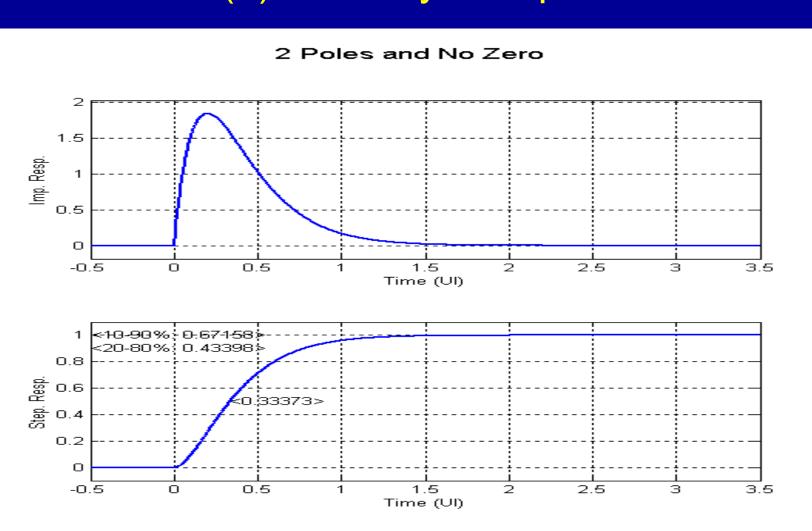


Case Study II: 2-Pole, 0-Zero (a) Under Damped

2 Poles and No Zero

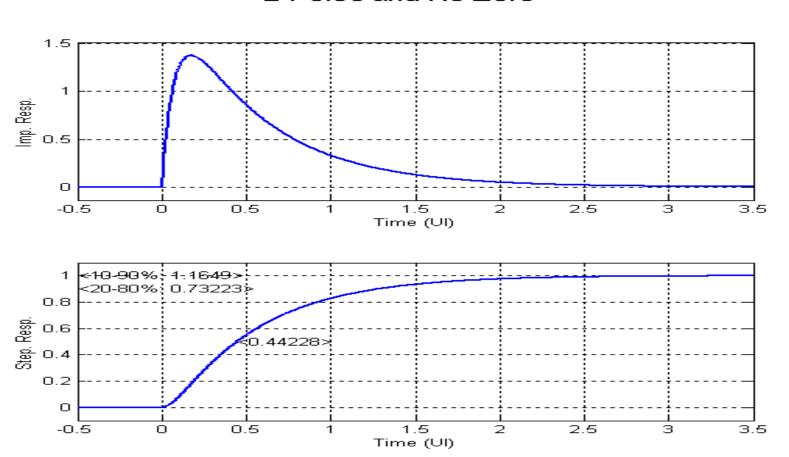


Case Study II: 2-Pole, 0-Zero Cont.. (b) Critically Damped



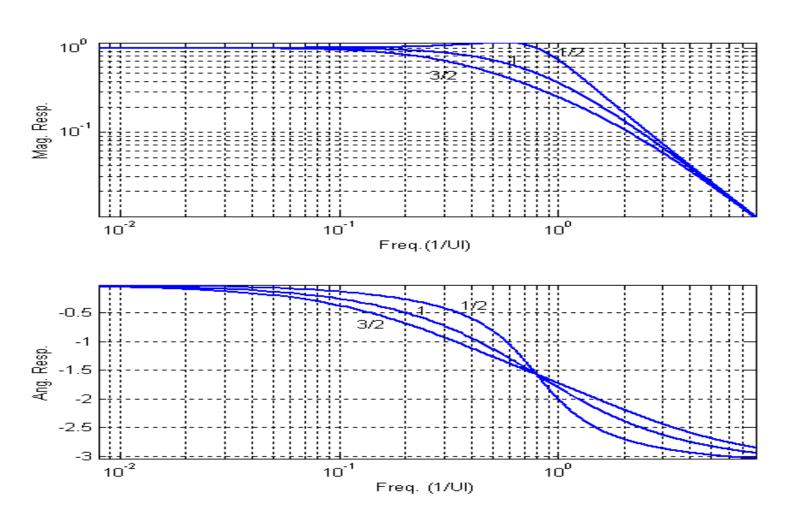
Case Study II: 2-Pole, 0-Zero Cont.. (c) Over Damped



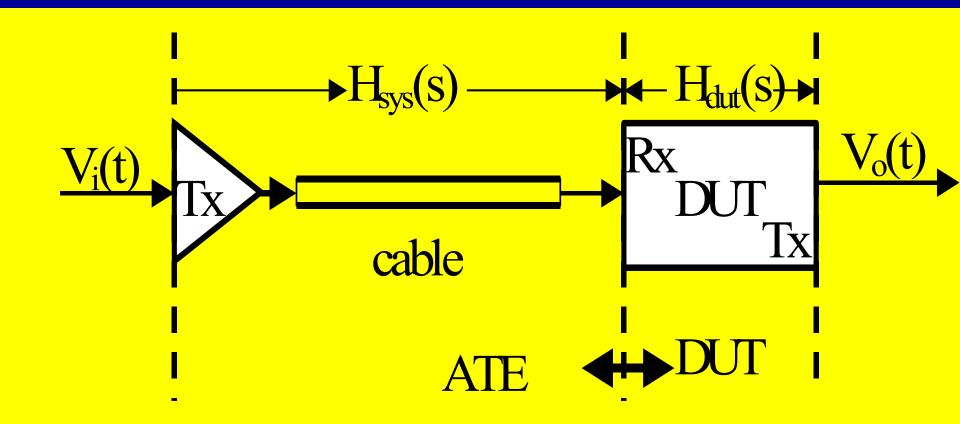


Case Study II: 2-Pole, 0-Zero Cont..

2 Poles and No Zero



Application to ATE DUT Path



Modeling Setup

$$H_t(s) = H_{sys}(s) \bullet H_{dut}(s)$$

$$h_{t}(t) = L^{-1}(H_{t}(s)) = \frac{1}{2\pi j} \int_{\sigma-j\omega}^{\sigma+j\omega} H_{t}(s)e^{st} ds$$

$$V_{0}(t) = h_{t}(t) * V_{i}(t)$$

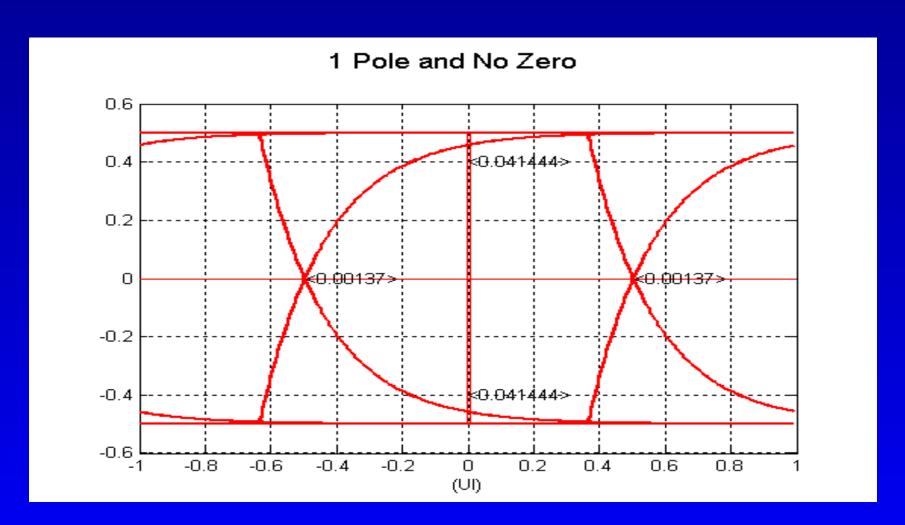
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Condition Settings

- H_{dut}(s): assumed to be a 1st-order (1-pole), this is the baseline
- H_{sys}(s): can be a 1st-order or a 2nd-order (1-pole, or 2-pole)
- H_t(s): will be a 2nd-order or a 3rd-order (2-pole or 3-pole)
- V_i(t): Datacom (K28.5, PRBS, CJTPAT) testing patterns

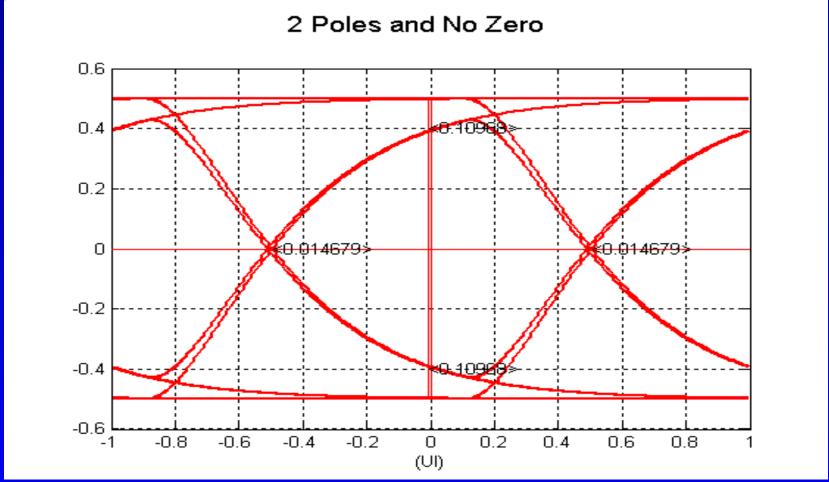
DUT Baseline Eye-Diagram

V_i(t): K28.5, H_{dut}(s): 1st-order (~ 1 UI Settling)



Effects of "Bandwidth"

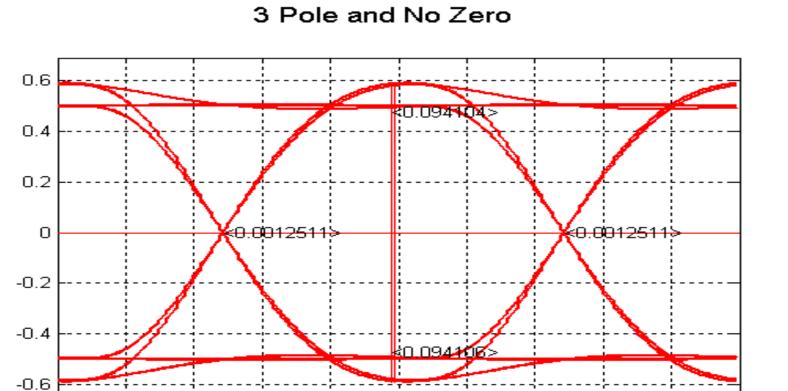
V_i(t): K28.5, H_{dut}(s): 1st –order (~1 UI settling),
 H_{svs}(s):1st –order (~2 UI settling)



V_o(t) eye-diagram

Effects of Ringing

 V_i(t): K28.5, H_{dut}(s): 1st –order (~1 UI settling), H_{sys}(s): 2nd –order (~2 UI settling)



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(UI)

0.2

0.4

0.6

0.8

-0.2

-0.4

-0.8

-1

-0.6

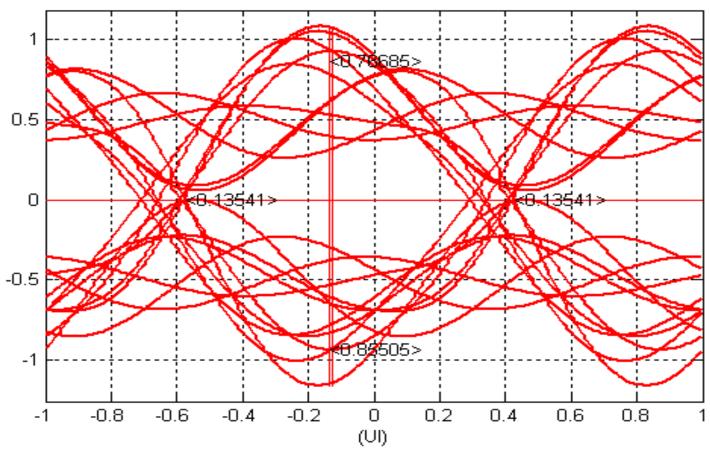
Summary Table for "Bandwidth" and Ringing Effects

	DUT	Effect of ATE "Bandwidth"		Effect of ATE Ringing	
		Total	ATE Induced	Total	ATE Induced
Timing ISI (UI)	0.0014	0.015	0.014	0.0013	-0.001
Voltage ISI (UA)	0.041	0.11	0.11	0.095	0.07

Effects of Data Pattern: K28.5

• $V_i(t)$: K28.5, $H_{dut}(s)$: 1^{st} – order (~ 1 UI settling), $H_{sys}(s)$: 2^{nd} –order (~ 8 UI settling)

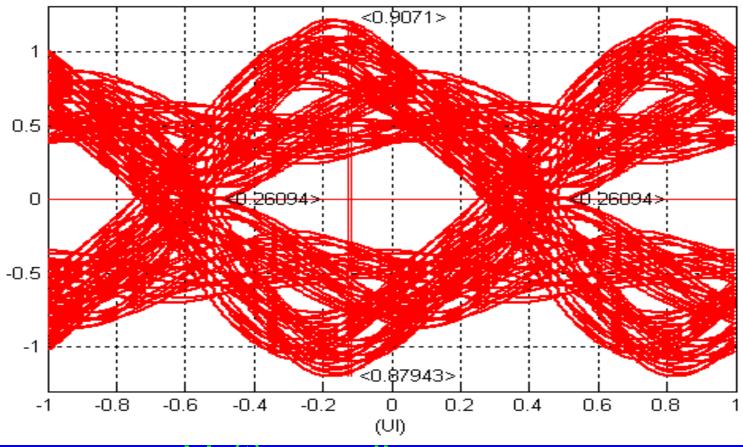
3 Pole and No Zreo



Effects of Data Pattern: PRBS210-1

• V_i(t): PRBS2¹⁰-1,H_{dut}(s):1st – order (~ 1 UI settling), H_{sys}(s): 2nd –order (~8 UI settling)

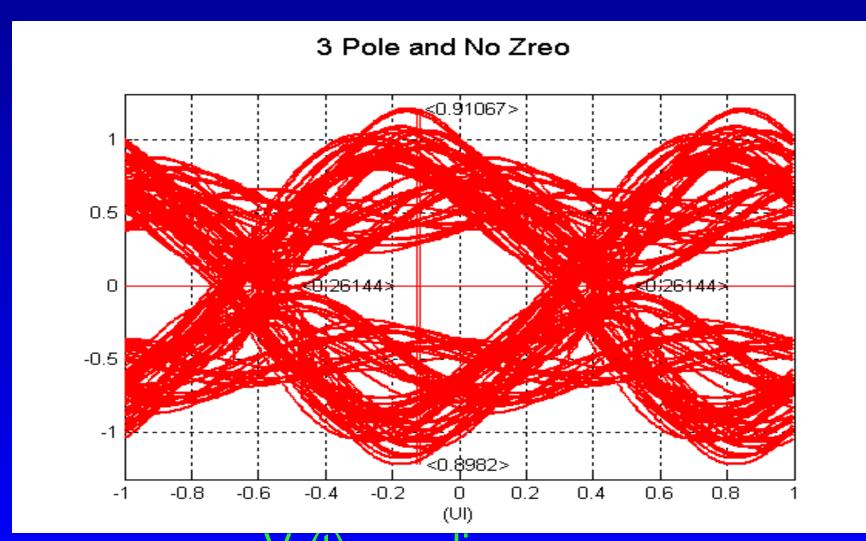
3 Pole and No Zreo



V_o(t) eye-diagram

Effects of Data Pattern: CJIPAI

• Vi(t): PRBS2¹⁰-1, H_{dut}(s):1st – order (~1 UI settling), H_{sys}(s): 2nd –order (~8 UI settling)



ummary Table for Different Pattern Effec

	K28.5	PRBS 2 ¹⁰ -1	CJTPAT		
Timing ISI (UI)	0.14	0.26	0.26		
Voltage ISI (UA)	0.86	0.91	0.91		

Summary and Conclusion

- A generic Nth-order (or N-pole, M-zero) model is established
- The generic model *eliminates* all the limitations of the simple, commonly used 1st – order (1-pole) model (see references in the paper)
- Scalability and completeness aspects of the generic model are demonstrated
- Application of the generic model in Datacom ATE
 I/O path is illustrated
- Simple 1st order model does not offer completeness and accuracy for high-speed Datacom ATE, and the generic model does