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Will “Heisenberg Uncertainty Principle” Hold For Designing and Testing Multiple GB/s ICs ?

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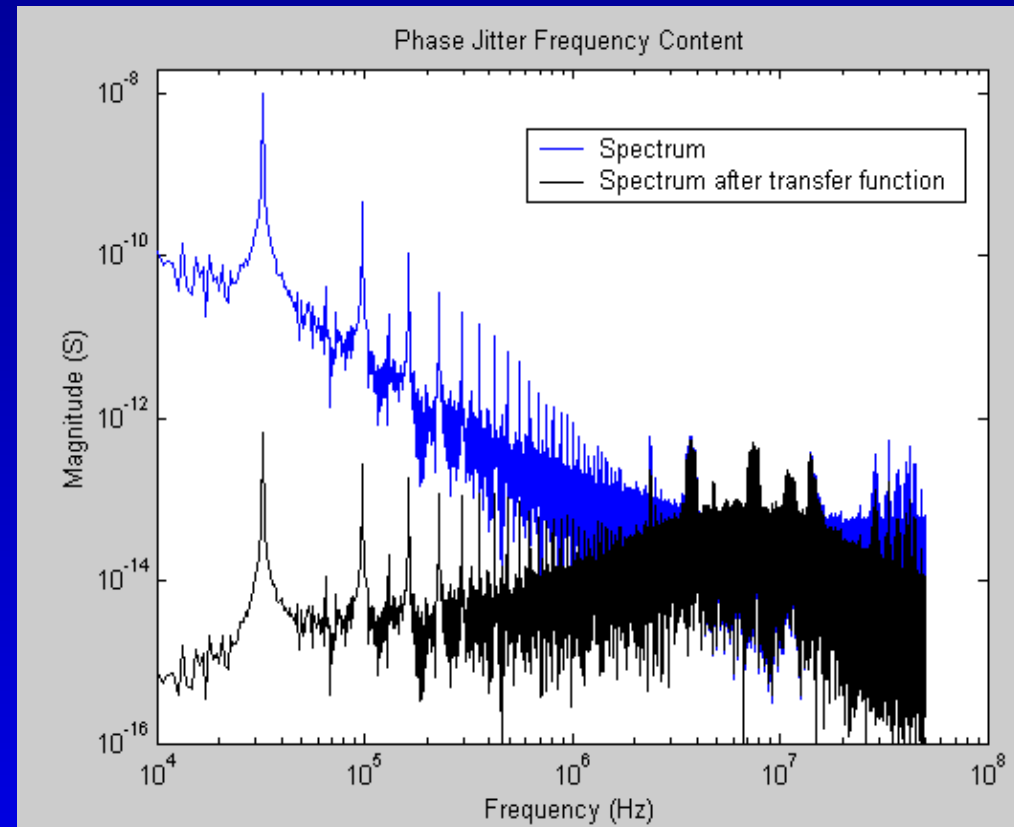
Outline

- Implications of low-cost, high performance, and, high volume
 - I.) lower cost
 - II.) design margin
 - III.) process technology
 - IV.) BER $\leq 10^{-12}$
- Summary and conclusion

I. Lower Cost Implications for Jitter

Lower Cost

- ◆ Cheaper component with ***a lot of intrinsic jitter*** (i.e, oscillator, clock generator, CMOS process, ect.)
- ◆ Limited power ***prevents driving fast edge***



Margin" Left

PCI Express System Jitter Budget

Components *barely* meet the system jitter requirements

Budget is so tight that non-linear *convolution* based system jitter distribution method needs to be used replacing linear sum method

Jitter Dis	Min Rj rms (ps)	Max Dj (ps) P-P	Tj at BER 10^{-12} (ps)
Tx	2.8	60.6	100
Ref Clock	4.7	41.9	108
Media	0	90	90
Rx	2.8	120.6	160
Linear Total Tj:			458
Root Sum Square (RSS) Total Tj:			399.13

III. CMOS Process Implications

- Process variation -> wide range of device parameters -> wide range of jitter distribution (i.e., PLL 3 dB can vary up to **12±10 MHz**, corresponding to **a few 10ps** jitter range)
- Multiple channel (up to ~ **100**) on a single chip intensifies the **crosstalk**
- Higher **corner frequency** of the 1/f noise for small feature size CMOS process technologies

IV. BER= 10^{-12} to 10^{-15}

- JNB is a statistical process
- 10^{12} to 10^{15} jitter and/or noise samples
- Very long (many hours) in-situ design simulation and/or testing time
- What price do we pay if we shortcut the statistical sample:?

Liability and/or yielding !!!

Summary and Conclusion

- *Penalty price will apply* if *JNB test is skipped* from from design to manufacture given the *low cost, high performance ($BER=10^{-12} - 10^{-15}$)*, and *high volume* requirements for Gbps ICs/systems.
- “Heisenberg Uncertainty Principle” *will continue hold* for JNB test