Characterization and Production Testing At 3.2-5.0 GB/s for PCI Express II and FB DIMM

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Abstract

In this paper, the architecture and test requirements for PCIe II and FB DIMM are reviewed. Solutions meeting those requirements will be demonstrated. We will highlight and emphasize those new test requirements such as minimum pulse width, deterministic jitter (DJ), full-swing and de-emphasized eyes, reference clock jitter, peaking and 3 dB corner frequency for PLL's, for PCIe II and FB DIMM. Finally, we will demonstrate how testing to a BER of 10^{-12} in less than 100ms is possible and how to maintain consistency and correlation between test results from design characterization to high volume production. These new test methodologies will assure that quality devices are shipped at a 10^{-12} BER while keeping test cost low.

1. Introduction

Communication architectures are moving to serial at data rates > 1 Gb/s due to their capability of delivering data at a rate up to 100 Gb/s and beyond. This serial link is an asynchronized system with a bit clock embedded in the transmitting data bit stream that is recovered at the receiver end of the link. The metric for quantifying the link performance is the bit error rate (BER). BER can be caused by either timing jitter and/or amplitude noise coming from the link components. For a copper based system, the major limiting factor is timing jitter. For a fiber based system, the limiting factors can be both timing jitter and amplitude noise. As the data rate continues to increase, jitter, noise, and BER (JNB) testing becomes a must in order to ensure high quality/performance for both the link system and devices within it.

The amount of JNB highly depends on the specific link system architecture as well as the link components such as transmitter, receiver and medium. The high-speed serial architecture was first implemented in long (~1 km < L < 1000 km) and medium range (~1 m < L < 1000 m) networks enabling applications such as SONET, Fibre Channel (FC) and Gigabit Ethernet (GBE). The architectures for these networks are relatively less complicated from the jitter transfer function point of view since the high performance devices and components can be used in these links due to the economic reasons while there is less jitter and noise to start with.

In recent years, however, serial communication architectures have been rapidly adopted and advanced in the shorter distance (L < 1 m) computer centric I/O links for applications such as PCI Express for microprocessor and chipset I/O links and FB DIMM for memory I/O links. The architectures for these I/O links are much more complex compared with earlier network serial links due to the concurrent high performance and low cost requirements. The key issue here is what kind of role does JNB play in this serial link system. No rational or accurate testing method can be developed until this role is clearly understood and quantitatively described.

At the same time, jitter, noise, and BER are different, yet related, statistical processes. This implies that all the statistical rules and theorems need to be complied with when testing them. In addition, because they are related, the interrelationship between them will provide useful guidelines and insights for deriving results from one type of process to another or to verify the correlation between them if two or three of those process measures are available. Clearly, the statistical nature of jitter, noise, and BER needs to be correctly combined with the system response of the link.

In section 2, we will first give an overview of the PCI Express II (5 Gb/s) and FB DIMM (3.2, 4.0, 4.8 Gb/s) architecture and related jitter transfer functions. Then we will review the test requirements and associated methods with a focus on JNB test for transmitter, reference clock, medium and receiver.

In section 3, we will demonstrate our testing solutions for covering both compliance and diagnostics test for those two standards. We will discuss the new testing requirements such as DJ, 3 dB bandwidth and peaking for PLL, reference clock phase jitter after a band-pass function, in addition to conversional testing parameters. The strategy for carrying correlated and consistent testing results from design characterization to high volume production will also be discussed.

In section 4 we will summarize and conclude.

2. Review of PCIe II and FB DIMM architecture and test requirements

2.1 PCIe II architecture and test requirement

PCIe II[1] is the second generation of PCIe link with data rate of 5 Gb/s which is twice as much as the data rate of generation I[2]. The unit interval (UI) is reduced from 400 ps to 200 ps. Clearly, the available jitter budget for each component will need to shrink down accordingly in order to meet the 200 ps UI limit.

The architecture of PCIe II is illustrated in Figure 1.

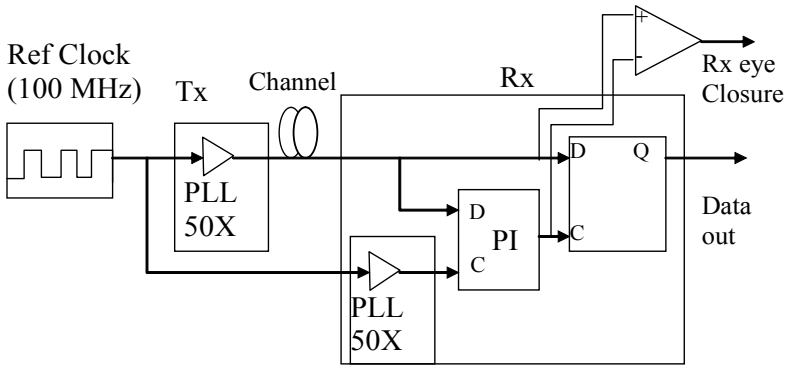

Figure 1. PCIe II link architecture diagram using a phase interpolator (PI) or an over-sampling (OS) in its receiver.

At the receiver, jitter and noise from link components of the transmitter, medium (channel), and reference clock will all contribute to the eye-closure from both time axis direction and voltage axis direction. The signal test (including both jitter and noise) will be composed of two parts: signal output tests and receiver tolerance tests. The signal output test includes both transmitter and reference clock signal output. We introduce the test requirements for each one in the following subsections.

2.1.1 Transmitter signaling test

2.1.1.1 Testing parameters

The key transmitter signal/jitter parameters to be tested are listed in the Table 2.1

Table 2.1: PCIe II Key Transmitter Test Parameters[1]

Symbol	Parameter and Definition	Gen I (2.5 Gb/s)	Gen II (5 Gb/s)	Unit
UI	Unit Interval	399.88 (min) 400.12 (max)	199.94 (min) 200.06 (max)	ps
VTX-DIFF-PP	Differential p-p Tx voltage swing	0.8 (min) 1.2 (max)	0.8 (min) 1.2 (max)	V
VTX-DE-RATIO -	Tx de-emphasis level	3.0 (min) -4.0 (max)	-5.5 (min) -6.5 (max)	dB
TMIN-PULSE	Instantaneous pulse width	Not spec'ed	0.9 (min)	UI
TTX-EYE	Transmitter Eye opening (@10^{-12} BER) including all jitter sources	0.75 (min)	0.75 (min)	UI
TTX-DJ-DD (max)	Tx deterministic jitter (DJ)	Not spec'ed	0.15 (max)	UI
BWTX-PLL	Maximum Tx PLL Bandwidth (BW)	22 (max)	16 (max)	MHz
BWTX-PLL-LO-3DB	Minimum Tx PLL BW for 3 dB peaking	3 (min)	8 (min) MHz	MHz
BWTX-PLL-LO-1DB	Minimum Tx PLL BW for 1 dB peaking	Not spec'ed	5 (min)	MHz
PKGTX-PLL1	Tx PLL peaking with 8 MHz min BW	Not spec'ed	3.0 (max)	dB
PKGTX-PLL2	Tx PLL peaking with 5 MHz min BW	Not spec'ed	1.0 (max)	dB
VRX-CM-AC-P	Rx AC common mode Voltage	150 (max)	150 (max)	mVP
RXSSC-JITTER-CC	SSC induced jitter that a receiver must track. Relevant only for common clock	Not spec'ed	65 ps PP at 33 KHz	ps
RXSSC-JITTER-SC	SSC induced jitter that a receiver must track. Relevant only for Tx only clock Architecture	Not spec'ed	20 ns PP at 33 KHz	ns

2.1.1.2 Testing requirements and methods

In order to test the transmitter signal as "seen" by the receiver, a clock recovery unit or function that emulates the receiver jitter tracking capability needs to be in place. A general transmitter signal/jitter output test setup is illustrated in the Figure 2.

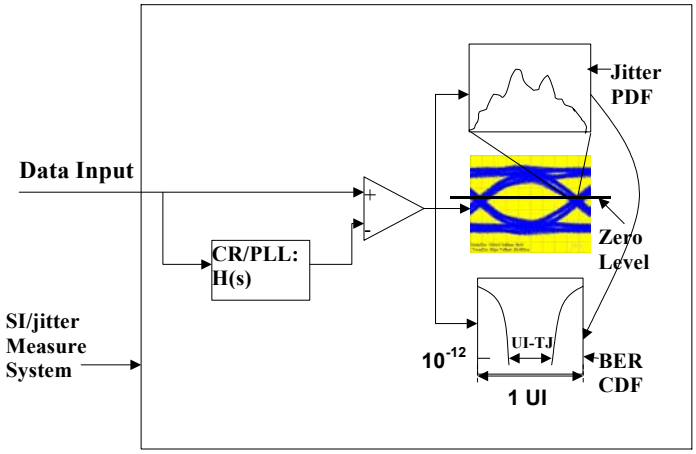

Figure 2. A schematic diagram shows the correct setup for JNB output testing.

The transfer function corresponds to PCIe II and is a 1st order high-pass function defined by the following equation (1):

$$H_3(s) = \frac{s}{s + \omega_3} \tag{1}$$

where ω_3 is simply $\omega_3 = 2\pi f_{3\_3dB}$, and f_{3_3dB} = 1 MHz is the 3 dB frequency. Figure 3 illustrates the shape of this 1st-order high-pass function.

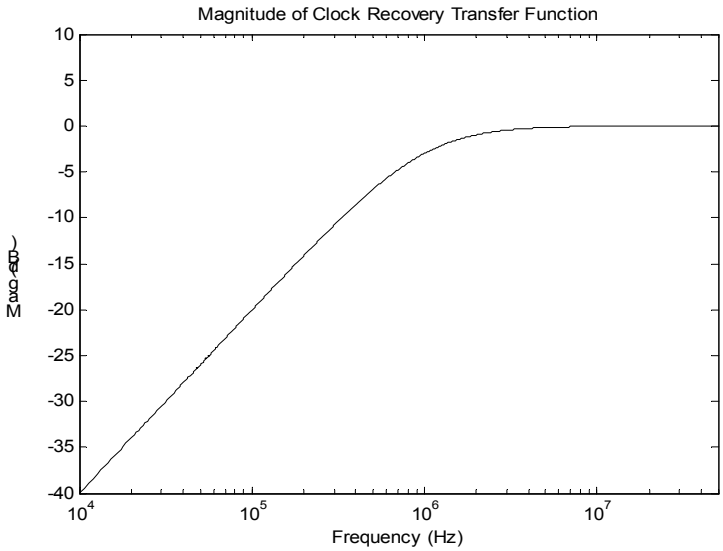

Figure 3. A graphical view of the 1st order high-pass function with a 3 dB frequency at 1 MHz.

This high-pass clock recovery function needs to be implemented for both jitter and eye-diagram output tests. It can be implemented by either a hardware clock recovery or a software clock recovery.

A transmitter compliance mask for both full swing and de-emphasis looks like the graph in Figure 4.

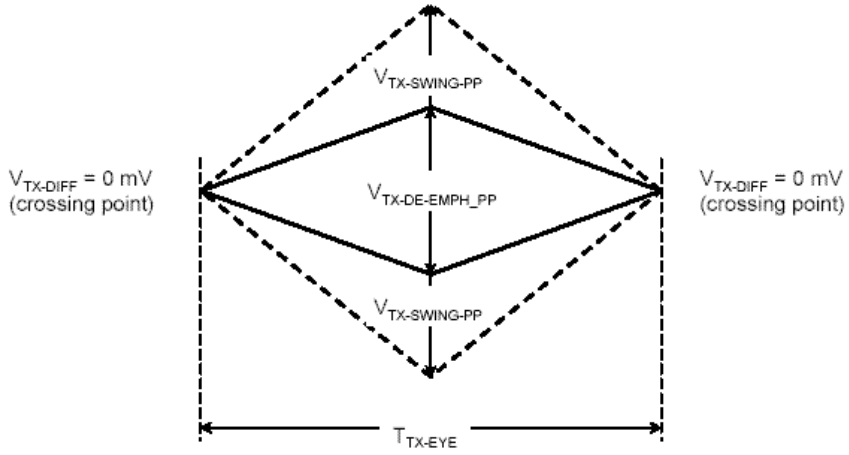

Figure 4. Transmitter compliance eye-masks for both full swing and de-emphasis bits.

These masks serve as "keep out" regions. Namely, if a voltage v(t) sample falls within those regions, then the device fails the compliance test.

2.1.2 Reference clock test

2.1.2.1 Reference clock testing parameters

In conjunction with the transmitter PLL, a 100 MHz reference clock will be used to generate an in-rate clock for transmitting data. In the case of the common clock architecture shown in Figure 1, this clock is also used with the receiver PLL for in–rate clock generation.

Table 2.2: PCIe II Key Reference Clock (100 MHz) Test Parameters[1]

Symbol	Parameter and Definition	Min	Max	Unit
TPERIOD-ABS	Averaged instantaneous period (including SSC)	9.997	10.053	ns
VIH VIL	Differential Input High Voltage Differential Input Low Voltage	+150	 -150	mV
VRB	Ring-back Voltage Margin	-100	+100	mV
$(dV/dt)_R$	Rising Edge Rate	0.6	4.0	V/ns
$(dV/dt)_F$	Falling Edge Rate	0.6	4.0	V/ns
η_{DC}	Duty Cycle	40	60	%
TCLK_RJ	Ref clk RMS jitter		3.1	ps
TSSC-JITTER-CC	SSC induced jitter that a receiver must track. Relevant only for common clock architecture		65 ps PP at 33 KHz	ps
TSSC-JITTER-DDC	SSC induced jitter that a receiver must track. Relevant only for data driving PLL architecture		20 ns PP at 33 KHz	ns

2.1.2.2 Reference clock testing methods

a.) Common clock architecture

Reference clock testing depends on the architecture of the PCIe link implementation. For the common-clock architecture, where the receiver uses PI or OS type of CDR method, its functional block diagram is shown in Figure 5,

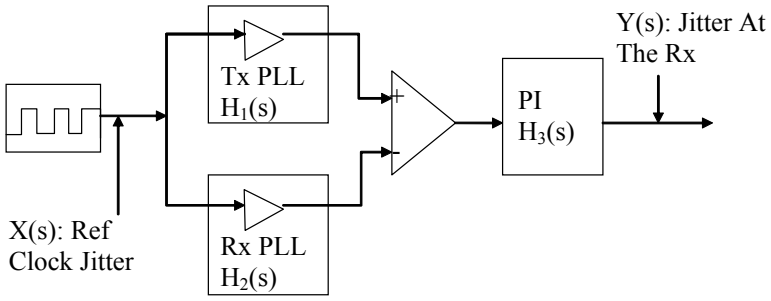

Figure 5. The transfer function diagram corresponds to common clock architecture.

The jitter relevant to the eye-closure at the receiver is given by the following equation[2]

$$Y(s) = H_t(s)X(s) = [H_1(s)e^{-sT_d} - H_2(s)]X(s) \tag{2}$$

where Td is the propagation delay between the paths to transmitter and receiver PLLs and X(s) is the phase jitter spectrum. The definition for H_1 and H_2 are given by:

$$H_1(s) = \frac{2\zeta_1\omega_{n1}s + {\omega_{n1}}^2}{s^2 + 2\zeta_1\omega_{n1}s + {\omega_{n1}}^2} \tag{3}$$

and

$$H_2(s) = \frac{2\zeta_2\omega_{n2}s + {\omega_{n2}}^2}{s^2 + 2\zeta_2\omega_{n2}s + {\omega_{n2}}^2} \tag{4}$$

.

The PLL parameters of natural frequency and damping factor for H_1 and H_2 are given in Table 2.3.

Table 2.3:Common Clock PLL Testing Parameters[1]

Symbol	Parameter and Definition	Min	Max	Unit
Td	Clock transport delay		12	ns
ω1	PLL #1natural frequency	4.31*2π or 1.82*2π		Mrad/sec
ζ1	PLL #1 damping factor	0.54 or 1.16		
ω2	PLL #2 natural frequency		8.61*2π	Mrad/sec
ζ2	PLL #2 damping factor	0.54 or 1.16		

b.) Transmitter only clock (or data driving PLL) architecture

For the transmitter only clock (or data driving PLL) architecture where the receiver uses PLL as its CDR method, its functional block diagram is shown in figure 6,

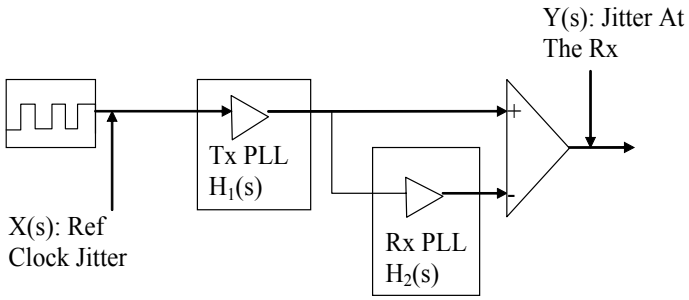

Figure 6. The transfer function block diagram corresponds to the transmitter only clock (or data driving PLL) architecture.

The jitter relevant to the eye-closure at the receiver in this case is given by the following equation:

$$Y(s) = H_t(s)X(s) = \{H_1(s)[1 - H_2(s)]\}X(s) \tag{5}$$

The PLL parameters of natural frequency and damping factor for H_1 and H_2 in this case are given in the Table 2.4.

Table 2.4: Transmitter Only Clock (or Data Driving PLL) Architecture PLL Testing Parameters[1]

Symbol	Parameter and Definition	Min	Max	Unit
ω_1	PLL #1natural frequency	4.31*2π or 1.82*2π		Mrad/sec
ζ_1	PLL #1 damping factor	0.54 or 1.16		
ω_2	PLL #2 natural frequency		50*2π	Mrad/sec
ζ_2	PLL #2 damping factor	TBD		

2.1.3 Receiver test

2.1.3.1 Receiver testing parameters

Table 2.5: PCIe II Key Receiver Test Parameters[1]

Symbol	Parameter and Definition	Gen I (2.5 Gb/s)	Gen II (5 Gb/s)	Unit
UI	Unit Interval	399.88 (min) 400.12 (max)	199.94 (min) 200.06 (max)	ps
VRX-DIFF-PP	Differential p-p Rx voltage swing	0.175 (min) 1.2 (max	0.120 (min) 1.2 (max)	V
VRX-MAX-MIN-RATIO	Max to Min pulse voltage on consecutive UI	Not specified	5 (max)	
TRX-MIN-PULSE	Instantaneous pulse width at Rx	Not specified	0.6 (min)	UI
TRX-EYE	Receiver Eye opening (@10^{-12} BER)	0.4 (min)	0.4 (min)	UI
TRX-DJ-DD (max)	Rx deterministic jitter (DJ)	Not specified	0.44 (max)	UI
BWRX-PLL-HI	Maximum Rx PLL Bandwidth (BW)	22 (max)	16 (max)	MHz
BWRX-PLL-LO-3DB	Minimum Rx PLL BW for 3 dB peaking	3 (min)	8 (min) MHz	MHz
BWRX-PLL-LO-1DB	Minimum Rx PLL BW for 1 dB peaking	Not specified	5 (min)	MHz
PKGRX-PLL1	Rx PLL peaking with 8 MHz min BW	Not specified	3.0 (max)	dB

In PCIe I, receiver tolerance test is not required. In PCIe II, receiver tolerance is required. The key requirement is that a receiver needs to have a BER=10^{-12} or better under the worst-case input signal conditions defined by Table 2.5. The following block diagram shows a worst-case eye-diagram receiver signal input condition, with various jitter component and appropriate spectral contents included.

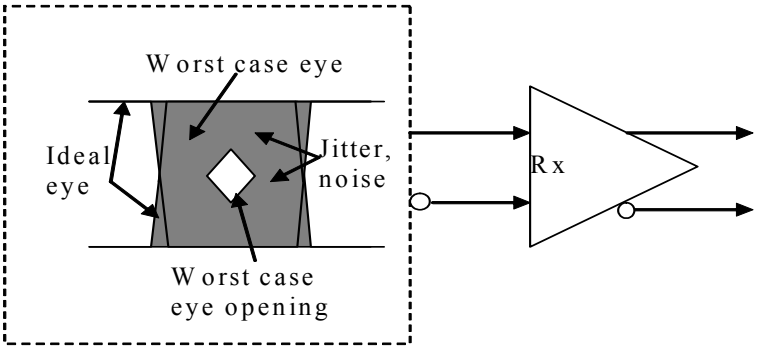

Figure 7. Worst-case eye/jitter signaling condition for receiver tolerance testing.

2.1.3.2 Receiver testing methods

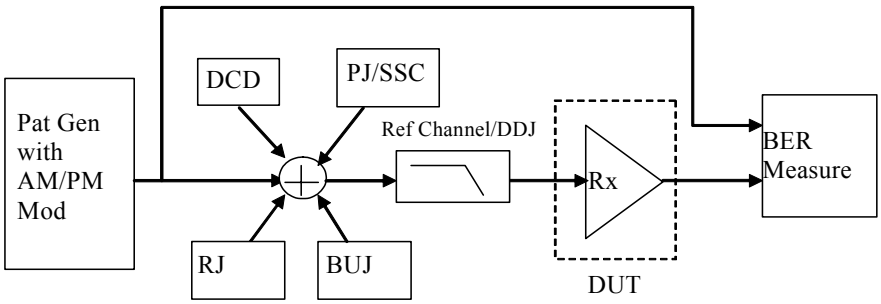

Figure 8. A generic jitter/signal tolerance testing method and setup illustration.

Figure 8 shows a generic receiver tolerance test functional block diagram. There can be several implementation methods to achieve the functional capability shown in this figure. In any case, the worst-case jitter/signaling condition given in Table 2.5 needs to be checked and verified before a receiver tolerance test can be made.

2.2 FB DIMM architecture and test requirement

FB DIMM[3] is a new high-speed I/O technology among advanced memory buffers (AMBs). It is largely driven by the local I/O data rate increase through technologies such as PCIe as well as the speed increase of microprocessors. Microprocessor, I/O and memory are three pillars for a computer system. If the goal is to advance the overall system performance, it is hard to leave one of them at the same performance level while the other two advance in their performance.

The rates of FB DIMM for its Generation I are at 3.2, 4.0 and 4.8 GB/s. Its architecture is quite similar to PCI Express I and II common clock architecture. As such, the testing requirements for FB DIMM are quite similar to PCIe II for its transmitter, reference clock and receiver. The major differences happen in the exact testing parameter thresholds.

The architecture of FB DIMM is illustrated in the Figure 9.

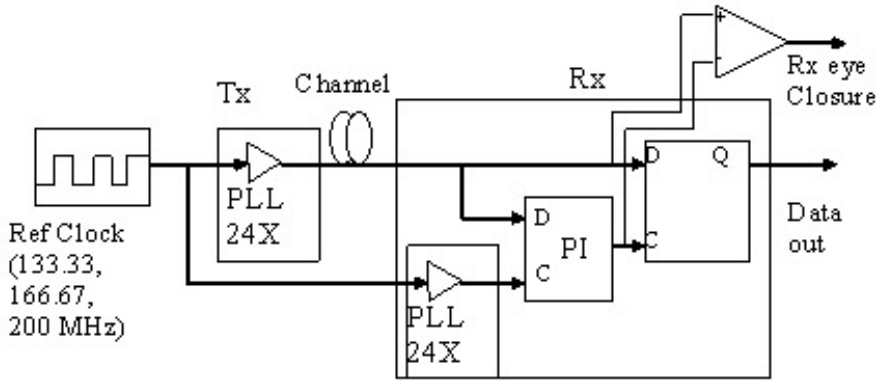

Figure 9. FB DIMM link architecture block diagram.

Notice that Figure 9 for FB DIMM is very similar to Figure 1 for PCIe II.

2.2.1 Transmitter test

The transmitter testing parameters for the FB DIMM are very similar to those introduced in 2.1.1.1 for PCIe II transmitter. We refer the readers to [3] for details. One major difference is that the CDR corner frequency for FB DIMM device is at ~ 200 KHz, much lower than that of PCIe II at ~ 1 MHz.

2.2.2 Reference clock test

Due to the similar architecture, FB DIMM reference clock test is very similar to that of PCIE II. In fact, FB DIMM reference clock test may be less complicated since it only needs to support the common clock architecture. Since the multiplication PLLs in both transmitter and receiver have the same multiplication factor (24X), the reference clock frequency will have to be different in order to achieve the three different data rates of 3.2, 4.0 and 4.8 Gb/s.

The reference clock jitter testing follows the same equation (2) for PCIe II in section 2.2.2.2 for FB DIMM but with different PLL and delay parameters. For FB DIMM, the PLL parameters used to determine the phase jitter for the reference clock are given in Table 2.6.

Table 2.6: F B DIMM PLL Parameters for Testing Reference Clock[3]

Symbol	Parameter and Definition	Min	Max	Unit
Td	Clock transport delay		5	ns
$\omega 1$	PLL #1natural frequency	5.92*2π		Mrad/sec
$\zeta 1$	PLL #1 damping factor	0.54	1.75	
$\omega 2$	PLL #2 natural frequency (3.2 and 4.0 Gb/s speeds)		17.2*2π	Mrad/sec
$\omega 2\text{-}4.8$	PLL #2 natural frequency (4.8 Gb/s speed)		11.8*2π	Mrad/sec
$\zeta 2$	PLL #2 damping factor	0.54	1.75	

2.2.3 Receiver test

Again, the receiver testing is very similar to PCIe II, except for the testing parameter thresholds. Various signal input parameters need to be checked and verified at the receiver input. At the same time, a BER $=10^{-12}$ receiver performance needs to be tested/verified under the worst-case signal and jitter conditions at the receiver input for the receiver tolerance test. All the jitter components need to be generated and meet the required spectral shape and content.

3. Case study example

In this section, we will present some testing examples for PCIe II running at a 5 Gb/s rate to illustrate how to carry out compliance test against its specification.

3.1 Transmitter test

3.1.1 Compliance test

Figure 10 shows the transmitter eyes (for both full swing and de-emphasize bits) and TJ tests.

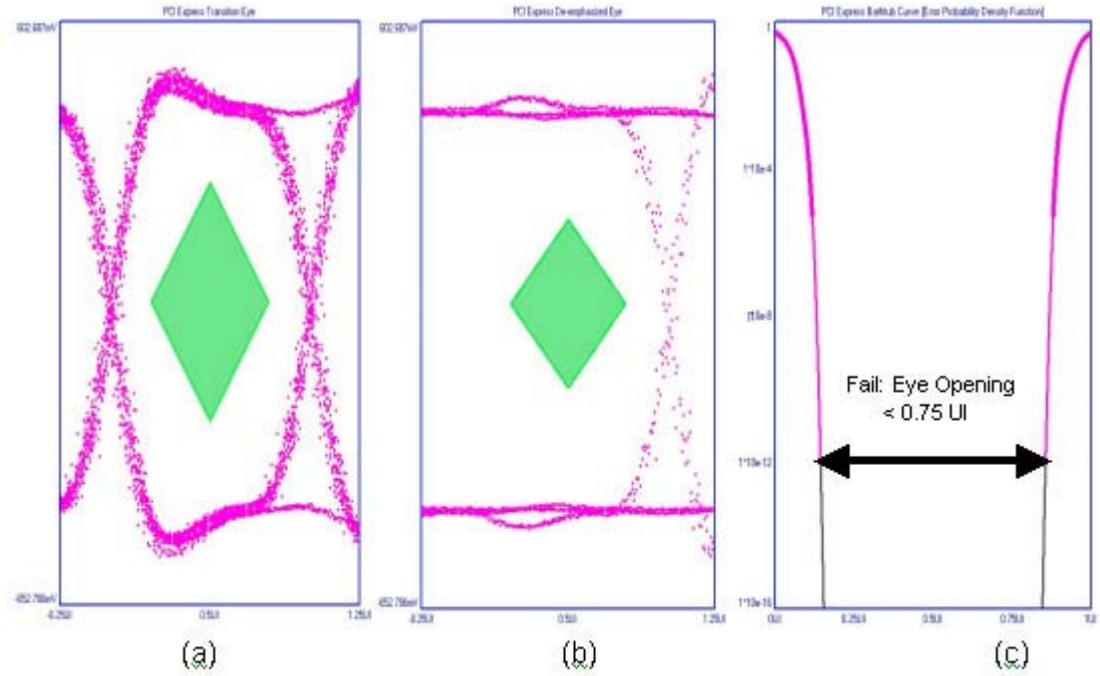

Figure 10. Transmitter signal/jitter output test results for its full-swing eye (a), de-emphasis eye (b), BER cdf (c) and associated TJ at BER= 10^{-12}.

In Figure 10, the eye-opening is 0.694 UI (or TJ =61.2 ps) for this transmitter. Therefore, this PCIe II transmitter marginally fails the compliance test. In the next section, we will discuss how to find out the causes for the failure.

3.1.2 Diagnostic test

Figure 11 shows the DDJ distribution, PJ and RJ power spectrum density (PSD) for the same transmitter that failed the compliance test in Figure 10.

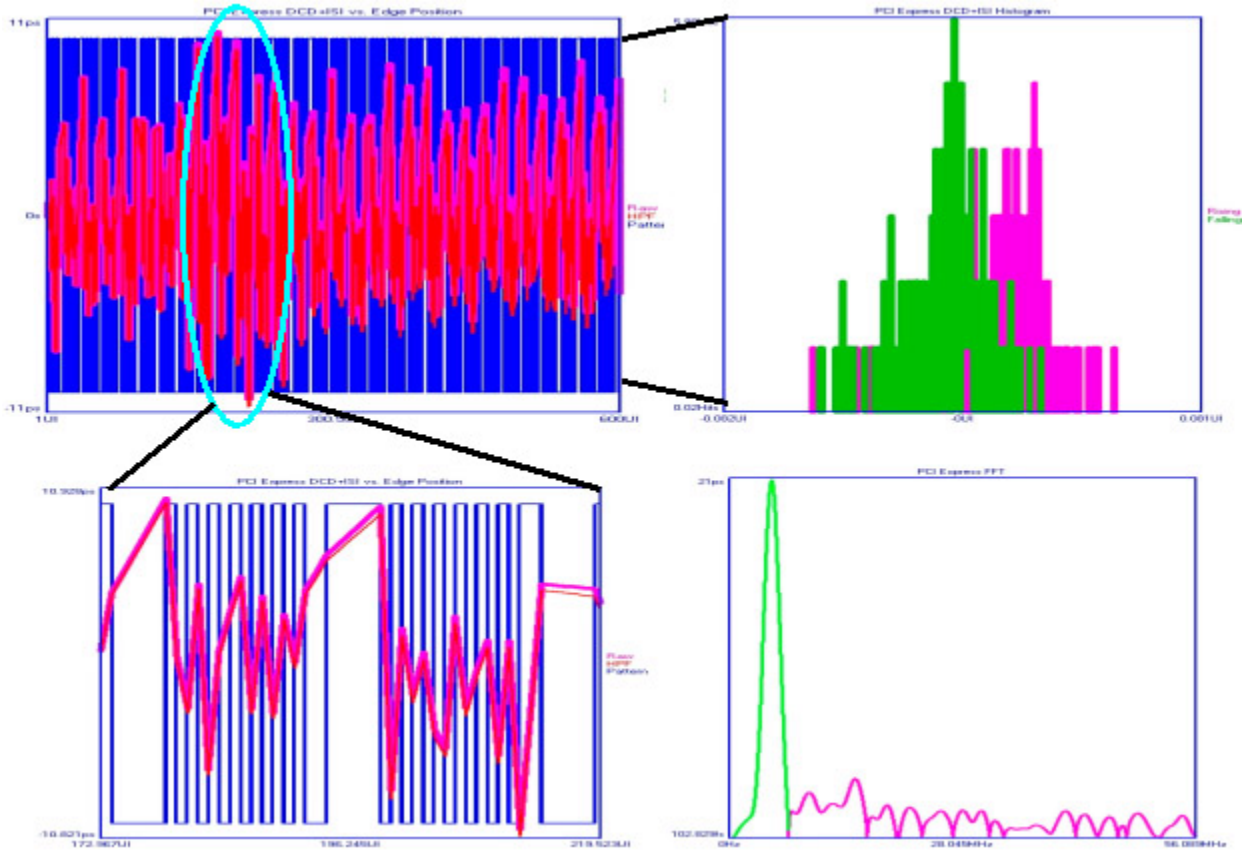

Figure 11. Transmitter jitter output diagnostic test results: a.) Upper left: DDJ as a function of UI span; b.) Upper right: DDJ histograms for rising (green) and falling edges (purple) respectively; c.) Lower left, zoom-in for those worst-case DDJ locations; d.) PSD shows both PJ and RJ power spectrum density shape.

It turns out that the major jitter contribution in this case is a PJ at 5 MHz with a magnitude of 20.9 ps. Had this PJ been removed, the transmitter would have easily passed the compliance test. The DDJ in this case is 20.7 ps while RJ rms is only 1.4 ps.

3.2 Reference clock testing

Figure 12 shows an example of a measured reference clock phase jitter before and after the jitter transfer function is applied. Those filter functions and estimation formulas are given by Eq. (2)-(4), with PLL parameters given in Table 2.4.

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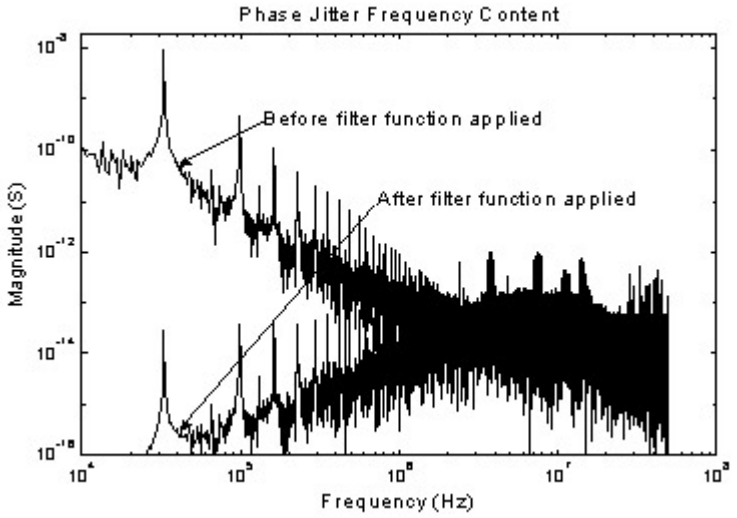

Figure 12. Reference clock phase jitter spectrum before and after the jitter transfer function is applied.

What we have obtained in Figure 12 is an s-domain spectrum, which only shows its magnitude part. The s-domain spectrum can be converted to a time-domain record by an inverse Laplace transformation with the results shown in Figure 13:

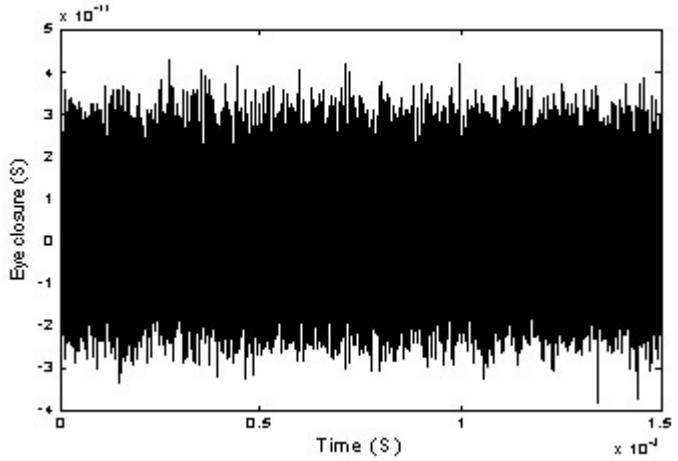

Figure 13. Time-domain phase jitter record after the jitter transfer function is applied

The RJ rms estimated from the data shown in Figure 13 is 8.31 ps and is larger than the specification limit of 3.1 ps. So, this reference clock fails the compliance test due to too much RJ generation.

3.3 PLL testing

The multiplication PLLs at both transmitter and receiver play important roles in determining the jitter seen at the receiver for the reference clock jitter. In fact, as it was shown in section 2, the estimations of transmitter, reference clock and receiver jitter performances all critically depend on the PLL characteristics termed by natural frequency and damping factor (or equivalently 3 dB frequency and peaking). Therefore, testing those PLL parameters are important and are required for PCIe and FB DIMM compliance specifications.

There are a few methods established to measure the transfer function and associated parameters for a PLL. One of them is a stimulus plus receiver where the stimulus is a pattern generator with phase or frequency modulation capabilities and the receiver is an oscilloscope. Recently, new receiver-only based PLL transfer function measurement methods have been developed that eliminate the need of using a stimulus and has much better throughput and cost advantages[4],[5],[6].

The requirements for PCIe II multiplication PLLs are shown in Table 2.1 for its transmitter and in Table 2.5 for its receiver. Figure 14 shows a few PLL measurement examples by using the variance function and no-stimulus method to measure PLL transfer function characteristics and related parameters such as peaking and 3 dB frequency.

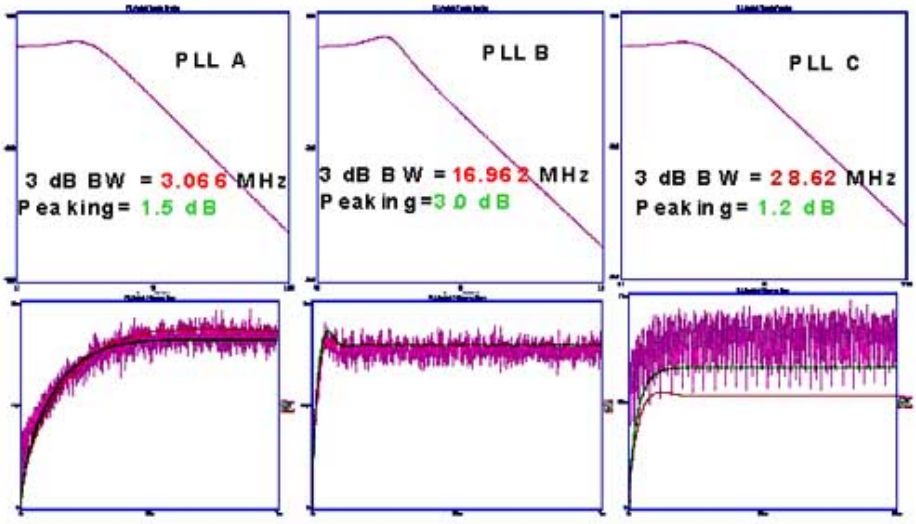

Figure 14: PLL transfer function measurement using a variance function, non-stimulus method for three PCIe II PLLs. 3 dB frequency and peaking are shown for each one.

In addition to transfer function, this variance-based, no-stimulus method also provides other parameters critical to PLL diagnosis and debug such as Bode plots, pole/zero location, pulling and locking parameters.

3.4 Testing from characterization to production

With the signal integrity analyzer (SIA) testing architecture[7], its ~ 1 ps accuracy, > million samples per second measurement rate and multiple parallel differential test channels, design characterization to high volume production test becomes easy and seamless for testing PCIe II and FB DIMM devices. The test times for most of the parameters required by those specifications introduced have been demonstrated to be less than 100ms with high confidence using the well-established autocorrelation and Tailfit jitter/signal analysis algorithms. Using the same hardware platform and test methodology from design to production removes the need of correlation between tests in those two phases, saving development time, overall time and reducing the cost for test.

4. Summary and conclusion

We have shown link architectures for PCIe II and FB DIMM and the corresponding compliance test parameters and associated testing methods for the transmitter, reference clock and receiver. Critical parameters such as transmitter deterministic jitter (DJ), total jitter (TJ) @ BER=10^{-12}, receiver clock and data recovery (CDR) jitter tracking function, PLL 3 dB frequency and peaking for both transmitter and receiver, reference clock jitter filter functions are discussed in great detail. We have shown that PCIe and FB DIMM have very similar architectures, test requirements and methods sharing significant synergies in terms of testing.

Finally, we illustrated practical case study examples for testing PCIe II devices running at 5.0 Gb/s. Transmitter compliance and diagnostic tests, reference clock compliance tests and PLL compliance tests are shown. The path for carrying signal/jitter testing from design characterization to high volume production using the Signal Integrity Analyzer (SIA) platform, along with its ~ps accuracy performance and < 100 ms throughput, is also discussed. Receiver tolerance tests are not covered in this paper but will be presented in a future publication. Those testing methods can be easily applied to other related serial link testing such as SATA/SAS, XAUI, Fibre Channel and Giga Bit Ethernet (GBE), and SONET.

References

[1] PCI Express Base Specification 2.0, Revision 0.7, PCI-SIG, 2005.

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