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Will “Heisenberg Uncertainty Principle” Hold For Designing and Testing Multiple GB/s ICs ?

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WAVECREST
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1. Introduction

At multiple Gb/s data rates, virtually all the communication architectures converge to serial where the clock timing is recovered at the receiver via various clock recovery schemes. While serial communication architectures and technologies were first developed and implemented in network centric communication systems that are characterized by relatively low volume, high cost, and high performance. However, continue pushing the same technologies to commodity applications such as personal computer (PC) will face severer challenges when cost and high volume constraints are imposed and the underline performance merit such as bit error rate (BER) is maintained at the same level of 10^{-12}. The economical version of "Heisenberg Uncertainty Principle" for the relationship between cost and performance will be in contradicting with the simple technology scaling approach, unless: a.) new technologies are developed to meet low cost, high volume, high performance requirements; b) cost and performance requirements are relaxed. In this paper, we will focus on specific challenges faced in design and test multiple Gb/s ICs when cost, performance, and volume constraints are imposed simultaneously, and discuss plausible solutions.

2. Lower cost -> higher jitter and noise

Under the cost constraint, the choices for the relevant technologies for designing and implementing transmitter, medium, receiver, and reference clock for a PC communication links such as PCI Express and Serial ATA at multiple Gb/s become very limited. The luxury of using expensive components having intrinsically low jitter is gone. For example, given the cost constraint for a typical reference clock of less than a few dollars, the clock selected for implementation will have significant amount of random jitter (RJ) and deterministic jitter (DJ). In another example, crosstalk will be significant due to up to 100 channels running simultaneously on a PC board with FR-4 traces. In a third example, transmitter edge rate (rise time and slew rate) can be limited thus it will result in large RJ; while achieving small RJ is possible by pumping in more power into the transmitter to drive fast edge rate but that will drive the cost up. The jitter and noise impacts to the receiver eye-closure will come from all the components used in the link, making the goal of maintain BER=10^{-12} difficult to achieve.

3. Design margin is hard to apply

The back of the envelope calculation indicates that the jitter budget is very tight for the link to the point that conventional and conservative linear summation jitter budgeting method (i.e., sum of total jitter (TJ) at BER=10^{-12} for all the subsystems of transmitter, medium, receiver, and reference clock being not more than 1 unit interval (UI)) is too simple and conservative, and a more advanced convolution based link jitter budgeting method needs to be invoked to gain some jitter margin for each component at the cost of knowing jitter components of DJ or RJ in addition to TJ. Design margin virtually does not exist given the cost and performance requirements at multiple Gb/s rate with channel number up to 100.

4. BER=10^{-12} drives long and comprehensive design simulation (DS) and design characterization & verification test (DCVT) processes

Jitter, noise, and bit error rate (JNB)[1],[2] is a statistical process. To handle JNB correctly, we have to follow the law of statistics and stochastic process. BER=10^{-12} implies a minimum 10^{12} edge transition samples that is astronomical relative to most of the DS and DCVT times encountered. When the channel number is included in the consideration, the number of samples required can increase to 10^{14} for 100 channels. While the model based extrapolation can cut down the sample size to a smaller number, say 10^{6}, but is at the cost of lower test coverage and confidence level due to that different JNB distributions at probabilities lower than the sample that a particular DS or DCVT process is taken caused by non-stationary processes such as low probability DJ, crosstalk, RJ drifting induced by equilibrium-state changing.

5. Process variation and zero design margin make it hard to ignore JNB in the high volume manufacture test (HVMT)

The low cost and high volume constraints lead to the CMOS process for manufacturing those devices where process variation is expected. For example, it is found that the 3 dB corner frequency for a second order phase-locked loop (PLL) used in transmitter and receiver can vary up to 10 MHz or more, result in TJ variation up to several 10 ps. Coupling with the virtually zero design margin, and BER=10^{-12} performance requirement, skipping JBN in HVMT is likely subject to penalties such as yield loss or liability.

6. Summary and conclusion

The nature of statistical JNB, low cost, high volume, and high performance requirements suggest that it is hard to skip JNB in any processes in designing and manufacturing multiple Gb/s commodity ICs. However, we certainly have room to improve in optimizing the relative role and cost for JNB in processes of DS, DCVT, and HVMT so that the overall cost will be minimized, similar to a conventional multiple variable optimization process. This approach may keep us away from violating "Heisenberg Uncertainty Principle". One example may be that JNB will be fully covered in DS and DCVT, but will be partially covered in HVMT for focused parameters/functions if that can result in the lowest overall cost.

References

[1] M. Li, "Production Test Challenges and Possible Solutions for Multiple Gb/s ICs", Proc. of International Test Conference, p. 1306, 2003.

[2] M. Li, "MultiGbps IC Test Challenges and Solutions", IEEE Design and Test of Computers, pp. 261-262, May-June, 2004.