Requirements, Challenges, And Solutions For Testing Multiple GB/s ICs In Production

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1. Introduction

As the data rate approaches 1 Gb/s and beyond, serial point-to-point communication with an embedded clock becomes the mainstream architecture. Such an architecture is traditionally used in the long-distance network and is now widely adopted in computer and peripheral links, in applications such as PCI Express, Rapid IO, XAUI, and Serial ATA, running at 1 to 10 Gb/s. Asynchronized IO, embedded clock, high volume, and low cost test solutions at > 1 Gb/s are new for a conventional synchronized production ATE system. This paper is intended to identify key challenges and to discuss possible solutions.

2. What need to be tested?

Communication ICs are generally merited by Bit Error Rate (BER). Most serial communication standards require BER at or below 10^{-12}. BER is a bottom-line number for a communication system determined by timing jitter and amplitude noise of the system. BER is also the cumulative distribution function (cdf) of the jitter/noise probability density function (pdf). Jitter test implies two different goals for transmitter and receiver. Jitter output for a transmitter should be upper bounded, while jitter tolerance for a receiver should be lower bounded. In summary, the most important function and/or parameters that need to be tested are:

- BER
- Jitter/noise (output for transmitter, tolerance for receiver)

3. Requirements for testing jitter /BER and related challenges

Testing a physical IC device always has two aspects: tester hardware and testing methodology. Jitter and BER testing are no exception. The overall testing system that is composed of both tester hardware (i.e., stimulus and/or receiver) and testing algorithm needs to ensure a best accuracy and repeatability so that optimal yielding/failing device rejection can be achieved, with high throughput. Bearing this as the overall goal, we discuss the requirements and related challenges in four different areas:

a.) Testing methodology/algorithm

Simple *deterministic* based testing method using only the overall peak-to-peak and rms values are no longer valid. Instead, *statistical* based method using pdf, cdf, deterministic jitter (DJ), random jitter (RJ), and total jitter (TJ) at a given BER needs to be employed.

Challenge #1: Most of the ATE production systems do not offer statistical based jitter/BER testing method.

b.) Hardware bandwidth and accuracy

Tester hardware, including both stimulus and receiver, needs to have very small DJ and RJ and high enough bandwidth. For jitter/noise analysis, tester hardware bandwidth needs to be close to the data rate frequency. For waveform analysis, a bandwidth of 3-5 times of the data rate is required. As an example: assuming a 10% total jitter margin at BER= 10^{-12}, 2% from DJ, and 8% from RJ, the DJ peak-to-peak and RJ rms of the tester should be less than those values in Table 1

Table 1: Tester DJ and RJ Requirements

	2.5 Gb/s	5 Gb/s	10 Gb/s
DJ pk-pk (ps)	8	4	2
RJ rms (ps)	2.28	1.14	0.57

Challenge #2: For a typical ATE system with 50 ps EPA, achieving DJ< 10 ps and RJ < 2.5 ps requirements are not trivial.

c.) "In-situ" testing

Serial data communication uses the recovered clock as the clock reference to recover the data at the receiver. This clock and data recovery (CDR) unit forms a high-pass frequency response that allows the receiver to track-off the low-frequency jitter, as well as constitutes the mask for the jitter tolerance test. Jitter frequency response function is a necessary element for testing jitter and BER. Without it, jitter/BER can be underestimated/overestimated.

Challenge #3: Most ATE systems do not have the CDR function built-in for testing serial transmitter/receiver.

d.) Throughput

Throughput for production is a critical merit. To catch one error with BER=10^{-12} for a 1 Gb/s link, it takes ~ 10^3 s. To enhance the statistical confidence, a bit error sample of 20 or so is needed. That means a good BER measurement with a BERT will take 2×10^4 s to complete, too long for any practical production test. In another example where an equivalent sampling scope is used for testing jitter via its eye-diagram function, it will take a few minutes to obtain timing jitter histogram with a few thousand hits.

Challenge #4: ATE systems equipped with BERT or sampling scope to test jitter/BER do not have the throughput advantages.

4. Possible solutions

In light of the complexity and difficulty level of those challenges, we believe that no single companies can solve all those challenges alone. If we look at the jitter/BER production test in conjunction with the lab characterization/test, we realized that testing methodologies, specialized high-performance (high bandwidth and small DJ and RJ) hardware, and CDR function have already been developed for lab applications. In short term, a logical solution will be to extend/integrate those proven technologies/IPs/solutions into the ATE production systems, solving the needs of time-to-market, easing the problem of lab to production correlation, and reducing the risk of solution development. Re-invent the wheel efforts are not cost effective for the end customers. With the open architecture system continue gaining the momentum, this extension/integration will become relatively easier.

In long term, higher level of integration of tester hardware, IP, and software has to happen to address the test cost issue. Other options need to be explored may include: BIST and DFT for internal or loop-back test. However, DFT and BIST for jitter/BER test is still in their infancy or research stage and practical solutions may not be available any time soon, given the analog nature of jitter/BER and most exiting DFT and BIST technologies are digital based.