An Introduction to Jitter Analysis
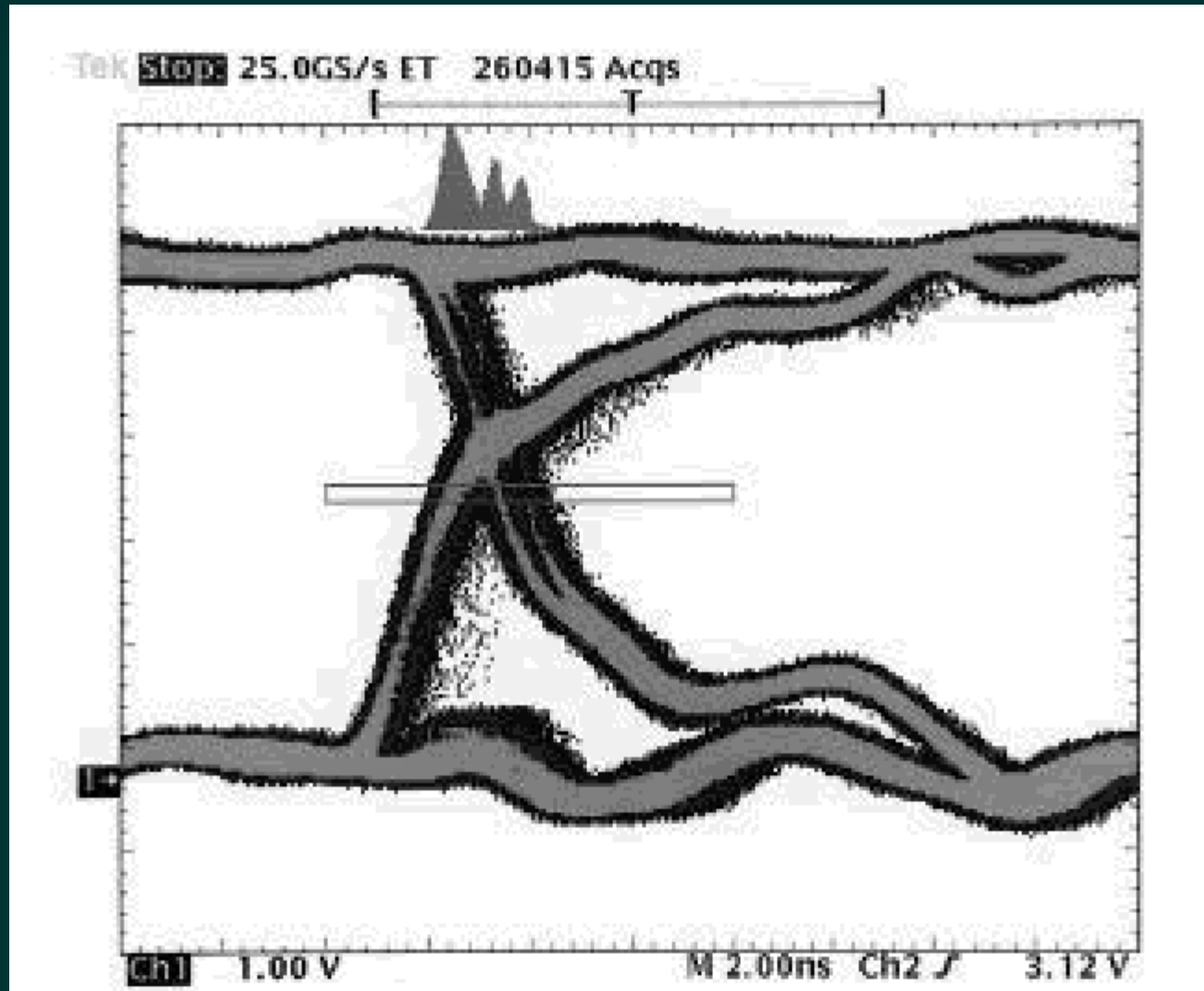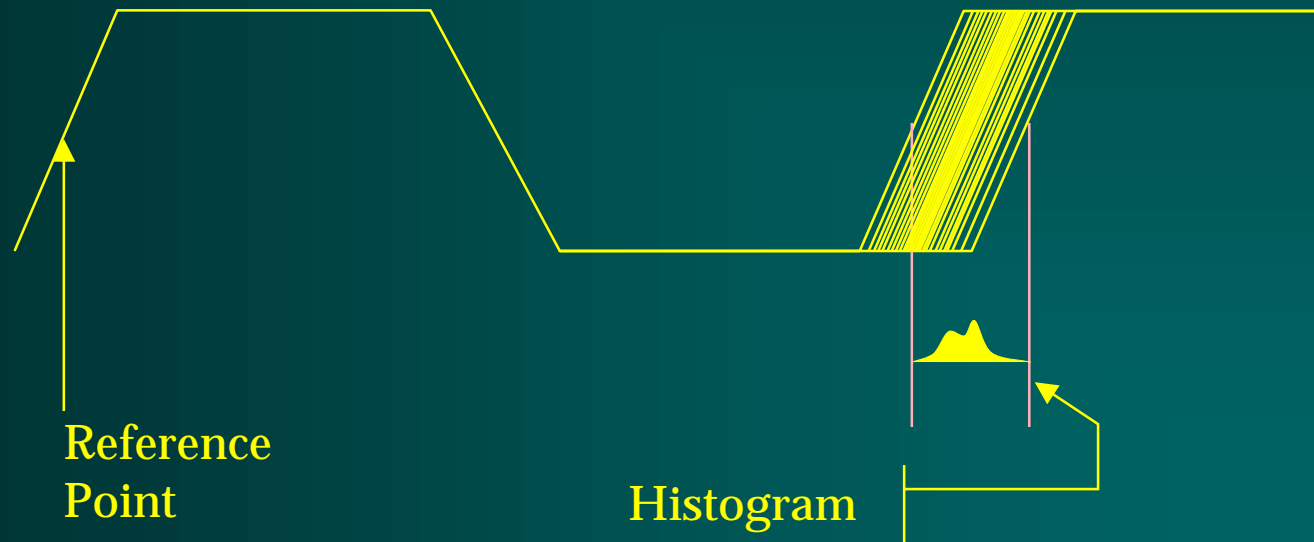
- **Jitter -**

  "The deviation from the ideal timing of an event. The reference event is the differential zero crossing for electrical signals and the nominal receiver threshold power level for optical systems. Jitter is composed of both deterministic and Gaussian (random) content."

  T11.2 / Project 1230/ Rev 10 Fibre Channel - Methodologies for Jitter Specification **page 7.**

Reference
Point

Histogram

What is Jitter Composed of?
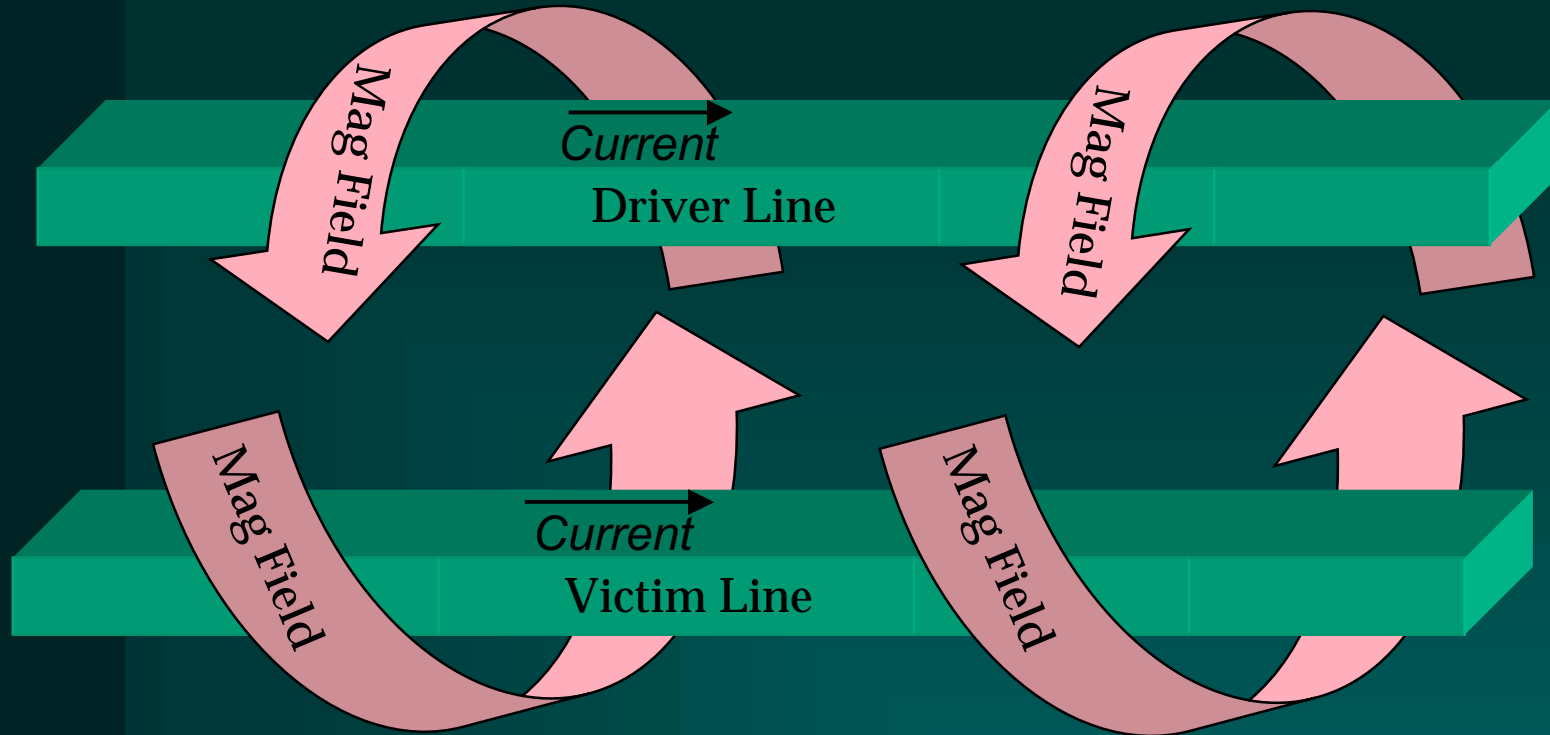
- ## Deterministic Jitter (DJ)

"Jitter with non-Gaussian probability density function. Deterministic jitter is always bounded in amplitude and has specific causes. Four kinds of deterministic jitter are identified: duty cycle distortion, data dependent, sinusoidal, and uncorrelated (to the data) bounded. DJ is characterized by its bounded, peak-to-peak value."

T11.2 / Project 1230/ Rev 10 Fibre Channel - Methodologies for Jitter Specification page 8.

- – DJ will never grow in amplitude regardless of the number of data points such that a sufficient number of data points were taken to complete at least one complete cycle of each periodic element.
- – Clock signals are typically susceptible to Duty Cycle Distortion (DCD) and Periodic Jitter.
- – Deterministic Jitter is typically caused by cross talk, EMI, Simultaneous Switching Outputs (SSO), device function dependency (pattern dependant jitter) and other regularly occurring interference signals.
- – Data signals are also susceptible to DCD and PJ as well as Inter-Symbol Interference(ISI) and Data Dependant Jitter (DDJ)

Where does DJ Come From?

Mag Field

Current

Driver Line

Mag Field

Mag Field

Current

Victim Line

Mag Field

- **Deterministic Jitter from Cross talk**
  – Victim line is affected by magnetic field from Driver line.
  – Incremental inductance of victim conductor converts induced magnetic field into induced current.
  – Induced Current adds (positively or negatively) to Victim Line current increasing or decreasing potential and thus causing jitter on Victim Line

Where does DJ Come From?

Switching Power Supply

Mag Field

Mag Field

Mag Field

Current
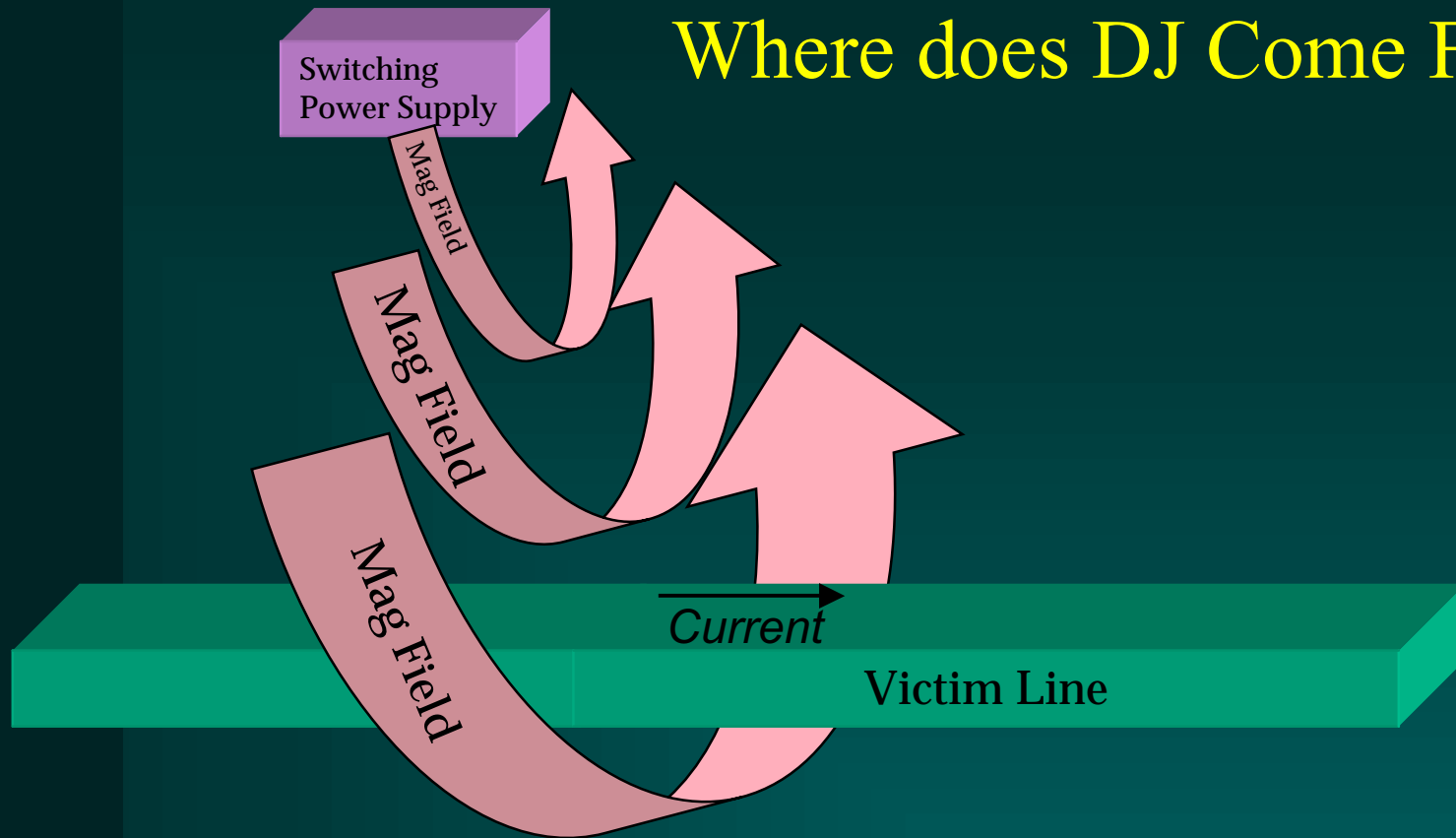
Victim Line

- **EMI Radiation (Ampere's Law)**
  - Victim line is affected by magnetic field from EMI Source. This could be a power supply, AC Power line, RF signal source, etc.
  - As in cross talk induced jitter, the magnetic field induces a current that is added (positively and negatively) to the victim line current thereby effecting the timing of the signal on the victim line.

Where does DJ Come From?

Vout

VCC

V_T

Vout

R_{OUT}

Edge Transition on the input to
the transistor

ΔV

ΔT
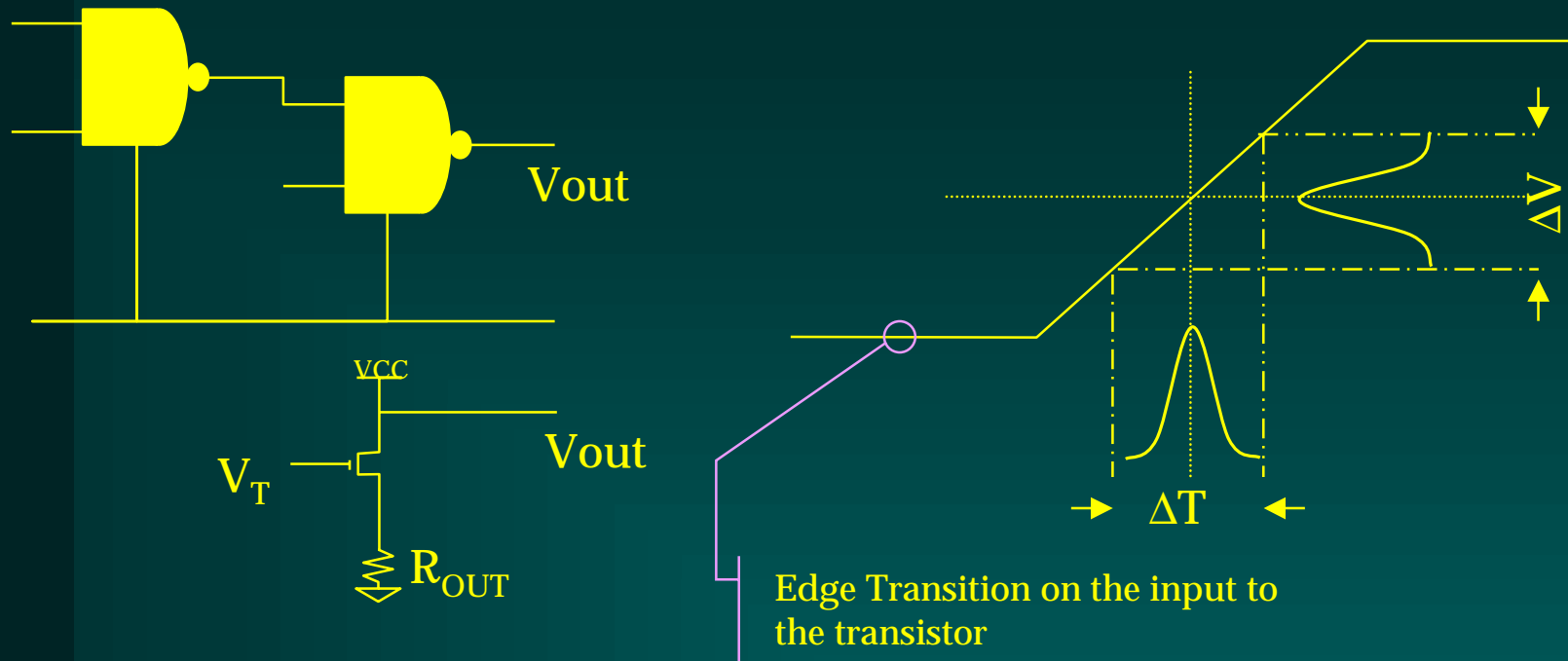
- ## Noisy reference plane
  - Noise in power planes can result in reference shifts in threshold voltages for downstream logic gates.
  - Resultant timing shift is proportional to slew rate of input signal.
  - The output transistor will switch when V_T is exceeded at the gate.
    - A change in ground reference at V_T will result in a shift in the required voltage to switch the gate thereby delaying or advancing the switch
  - VCO in PLL is sensitive to GND level variance.

Where does DJ Come From?
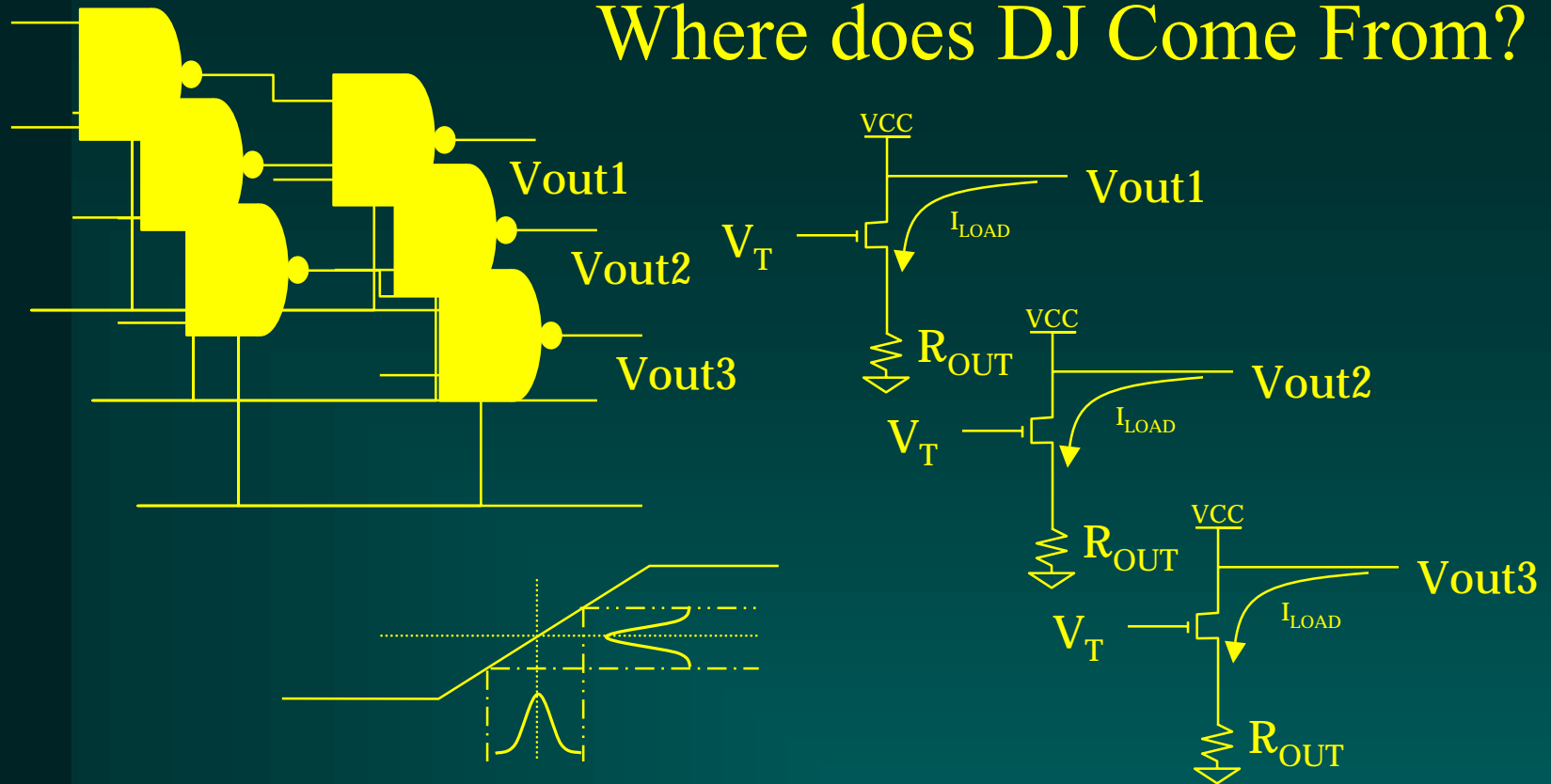
- ## Simultaneous Switching Outputs
  - If all output pins switch to same state, spike currents will be induced on VCC and on GND.
  - Spike Currents on Reference Plane can cause Threshold Voltage sense point to shift
  - Due to the pattern sensitivity and the bounded max. amplitude of edge jitter due to SSO, this is considered deterministic jitter.
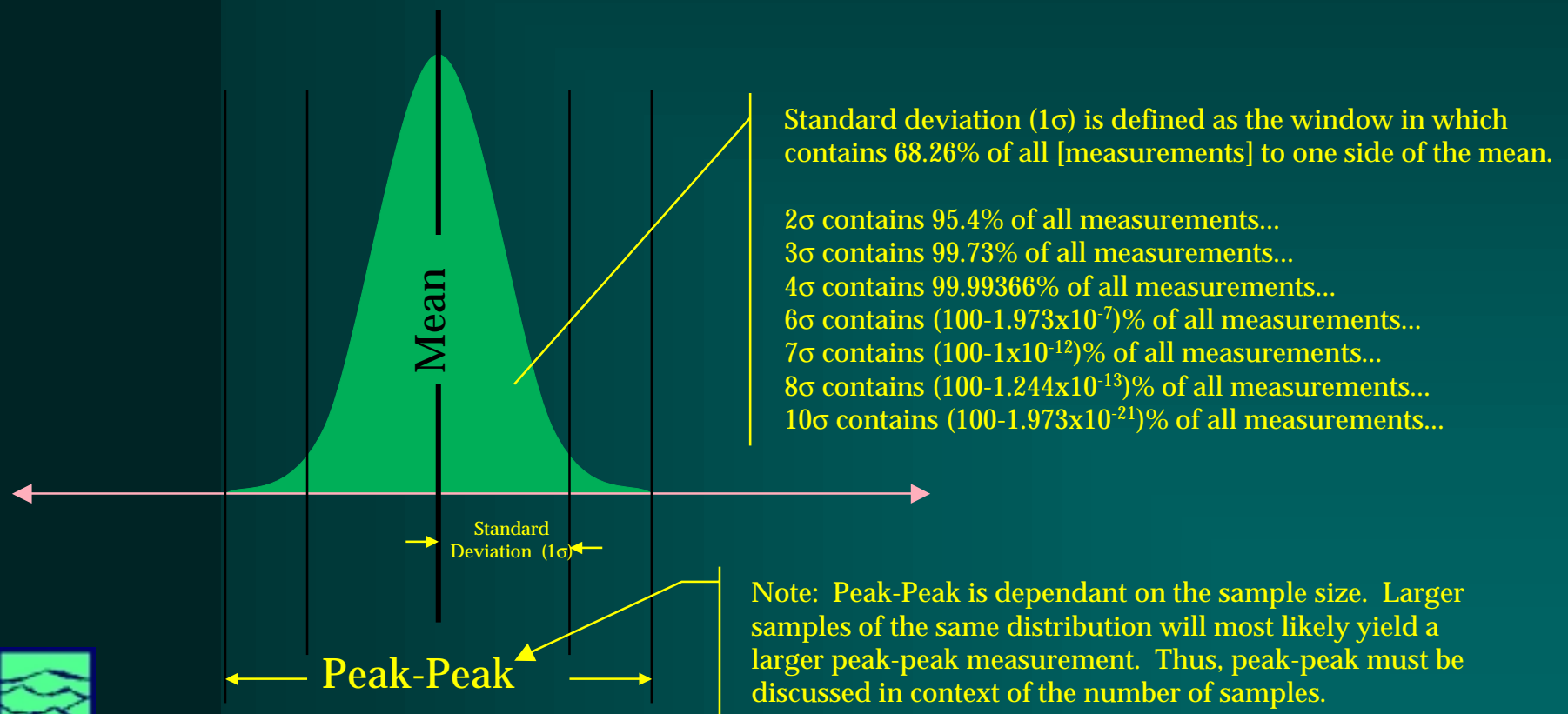
What else is Jitter Composed of?

- ## Random (Gaussian) Jitter (RJ) -
  - Like all physical phenomena, some level of randomness to edge deviation occurs in all electronic signals. This component is probabilistic in nature and is best modeled by a Gaussian function.
  - Random Jitter is unbounded and therefore directly effects long term reliability.

- ## Where does Random Jitter Come from?
  - Thermal vibrations of semiconductor crystal structure causes mobility to vary depending instantaneous temperature of material
  - Material boundaries have less than perfect valence electron mapping.
    - Imperfections due to semi-regular doping density through semiconductor substrate, well and transistor elements,
    - Imperfections due to process anomalies
  - Thermal effects of conductor material. Thermal vibration of conductor atoms effect electron mobility
  - And many more minor contributors such as:
    - cosmic radiation, etc...

What else is Jitter Composed of?

- ## Random (Gaussian) Jitter (RJ) -

  - Before we can talk about measuring Jitter, it is important to understand Gaussian Distributions as it relates to probability.

- ## Intro to Gaussian Distributions

Standard deviation (1σ) is defined as the window in which contains 68.26% of all [measurements] to one side of the mean.

2σ contains 95.4% of all measurements...
3σ contains 99.73% of all measurements...
4σ contains 99.99366% of all measurements...
6σ contains $(100\text{-}1.973\text{x}10^{-7})$% of all measurements...
7σ contains $(100\text{-}1\text{x}10^{-12})$% of all measurements...
8σ contains $(100\text{-}1.244\text{x}10^{-13})$% of all measurements...
10σ contains $(100\text{-}1.973\text{x}10^{-21})$% of all measurements...

Mean

Standard Deviation (1σ)

Peak-Peak

Note: Peak-Peak is dependant on the sample size. Larger samples of the same distribution will most likely yield a larger peak-peak measurement. Thus, peak-peak must be discussed in context of the number of samples.

More Gaussian Statistics

- ## Gaussian Statistics

  - It is important to note that in pure Gaussian mathematics, all possible measurements are assumed to be possible. However, for all practical purposes, the Gaussian model holds true in electronics for measurement populations not exceeding 10^{21}. This is equivalent to 20σ (single sided).

    - So, go ahead and use these Gaussian assumptions up to a reliability of about 20σ. After that, all bets are off as to the predictability of the measurement. 20s reliability implies compliant operation for at least 321,502.06 years for a 100MHz clock

Mean

Gaussian Distribution with small standard deviation

Gaussian Distribution with large standard deviation
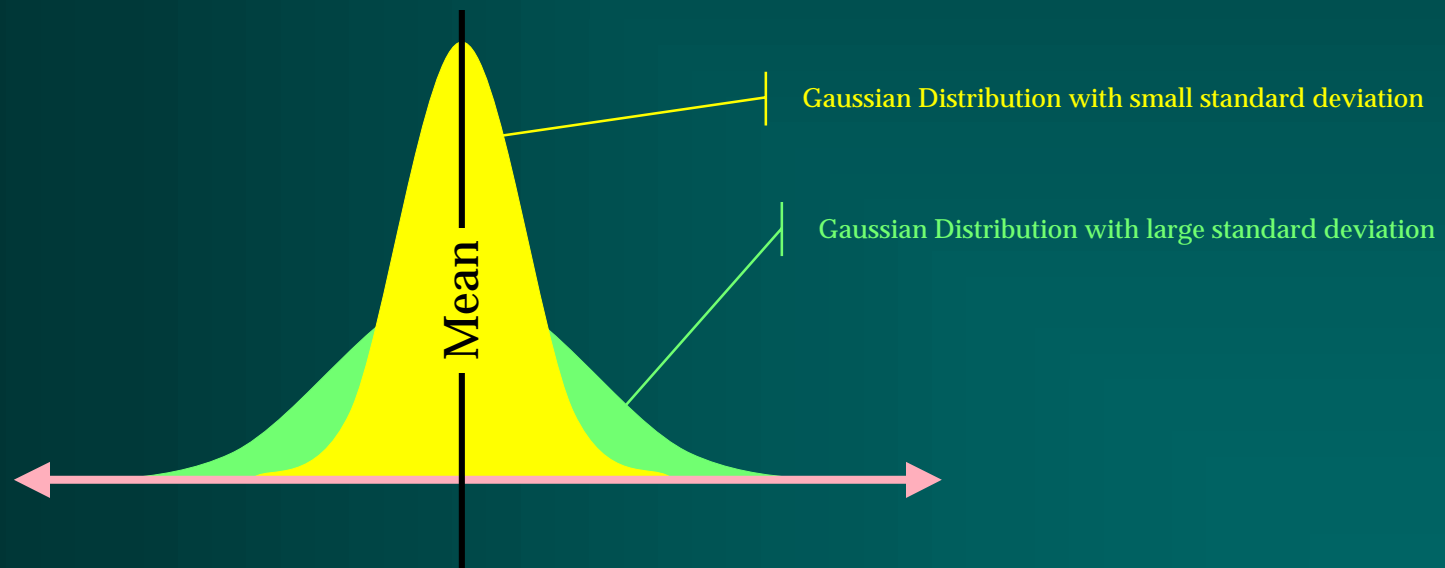
Why Standard Deviation?

- Standard Deviation is used to predict the occurrence of outlying measurements from the mean.

  - In electronics, it is important to know the frequency of occurrence of edges that are too early.

    - For example, if your system cannot tolerate clock periods that are less than 9.5ns on a 100MHz clock, you would like to know what the probability of a 9.5ns period is. Knowledge of the short period tail can tell you exactly how often a 9.5ns period occurs.

A measurement 2σ away from the mean will have a 95.4% chance of occurring. Thus, once every 250 periods, the period is less than (mean - $2*1\sigma$). If we use the numbers from the previous slide, once every 250 periods the period is less than 9.97ns.

MEAN

-2σ -1σ
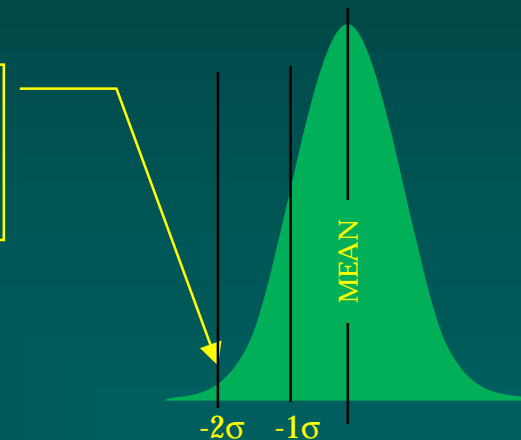
- The Catch…

  - This use of Standard Deviation (1σ) is only valid in pure Gaussian distributions. If any deterministic components exist in the distribution, the use of 1σ based on the entire jitter histogram for the estimation of probability of occurrence is invalid.

Calculating Standard Deviation

Measurements	
10.2ns	10.2ns
10.8ns	10.3ns
10.6ns	10.5ns
10.2ns	10.2ns
10.3ns	10.8ns
10.5ns	10.6ns

Standard Deviation $= \sqrt{\dfrac{1}{n-1} \sum_{i=1}^{n} (X_i - \overline{X})^2}$

where $\overline{X} = \dfrac{1}{n} \sum_{i=1}^{n} X_i$

$$\overline{X} = \frac{1}{12}(10.2+10.8+10.6+10.2+10.3+10.5+10.2+10.3+10.5+10.2+10.8+10.6) = 10.43ns$$

Std. Dev. $= \sqrt{\dfrac{1}{12-1} + \left(\begin{array}{l} (10.2\text{-}10.43)^2 + (10.8\text{-}10.43)^2 + (10.6\text{-}10.43)^2 + (10.2\text{-}10.43)^2 + (10.3\text{-}10.43)^2 + (10.5\text{-}10.43)^2 + \\ (10.2\text{-}10.43)^2 + (10.3\text{-}10.43)^2 + (10.5\text{-}10.43)^2 + (10.2\text{-}10.43)^2 + (10.8\text{-}10.43)^2 + (10.6\text{-}10.43)^2 \end{array} \right)}$
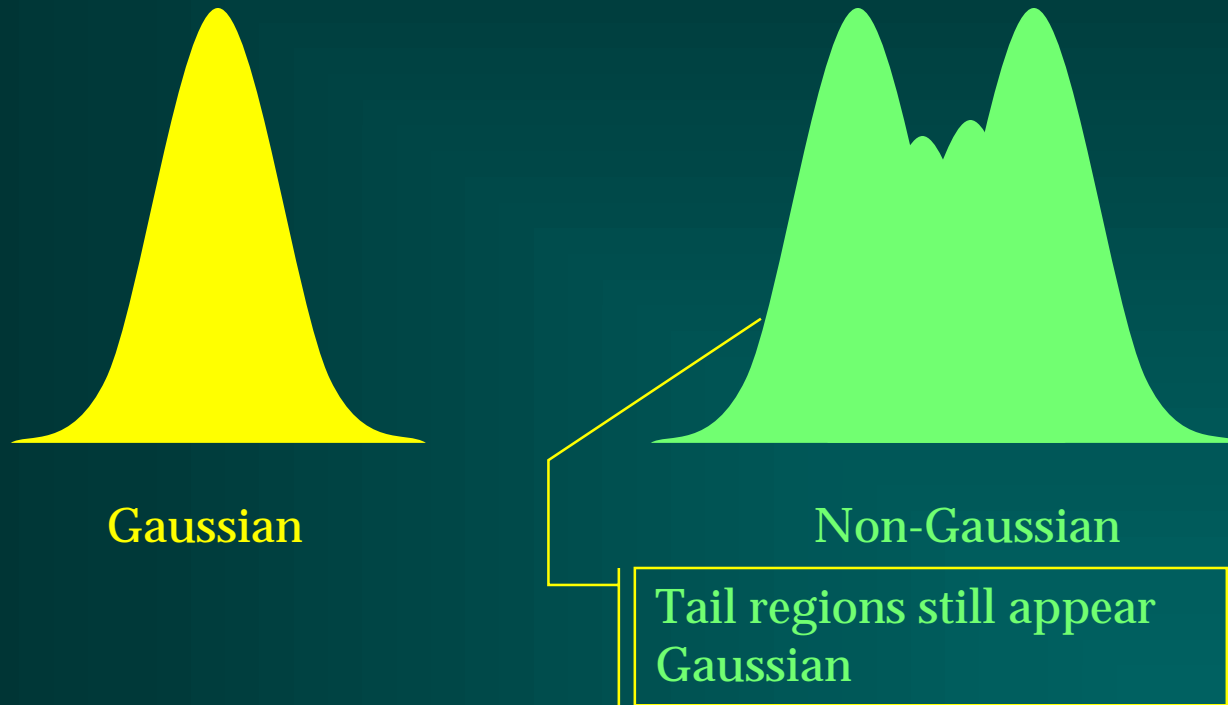
$= \sqrt{\dfrac{1}{11} + (.23)^2 + (.37)^2 + (.17)^2 + (.23)^2 + (.13)^2 + (.07)^2 + (.23)^2 + (.13)^2 + (.07)^2 + (.23)^2 + (.37)^2 + (.17)^2}$

$= .231ns$

"Real World" Distributions

- In most cases, time measurement distributions are not entirely Gaussian.
  - Typically, some Deterministic/Systematic offset occurs to "mess-up" the distribution to make it Non-Gaussian

Gaussian

Non-Gaussian

Tail regions still appear Gaussian

In non-Gaussian distributions, Gaussian assumptions apply to the tails (left most and right most regions) if and only if the equivalent 1σ of these tail region can be calculated.
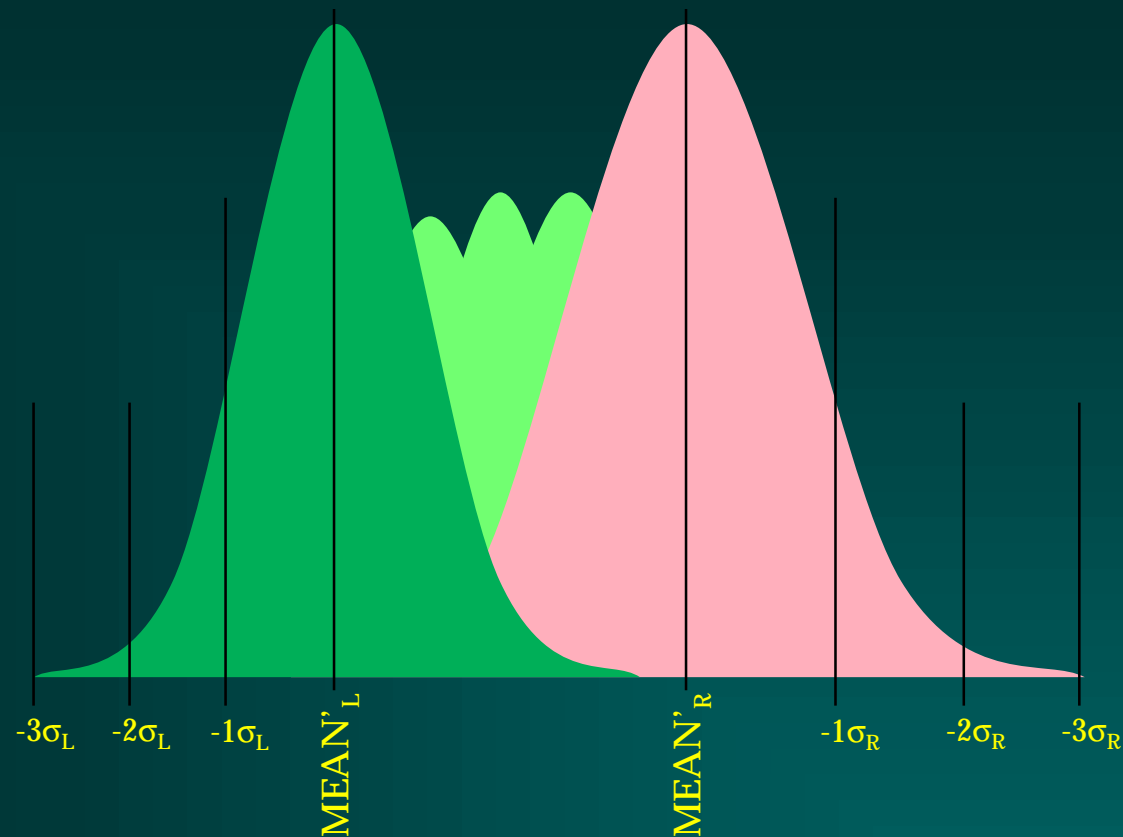
Non-Gaussian Distributions

Break up distribution
into tail and mid sections.

LEFT   RIGHT
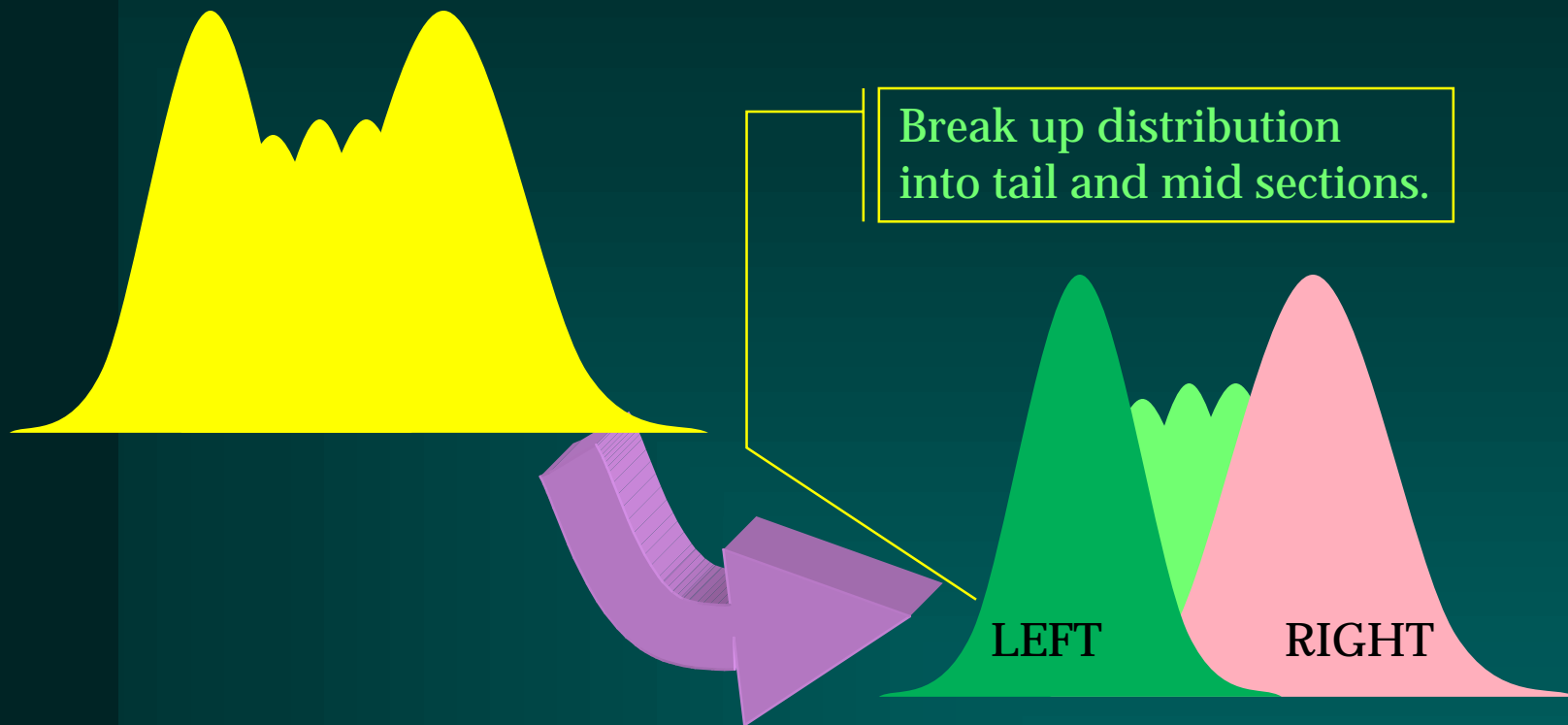
- Analyze distribution by looking at tail sections separately.
  – Allows for probabilistic estimations of out lying measurements
  – knowledge of Gaussian component (Random Jitter) on left side of multimodal
    distribution enables the calculation of the probability of short cycle measurements.
    • NOTE: Multimodal distributions are those distributions with more than one "hump". The non-Gaussian example
      shown here is referred to as bimodal. Some interesting information can be inferred from the shape of this
      distribution.   Symmetric peaks imply equal probability of either mean point (left or right).
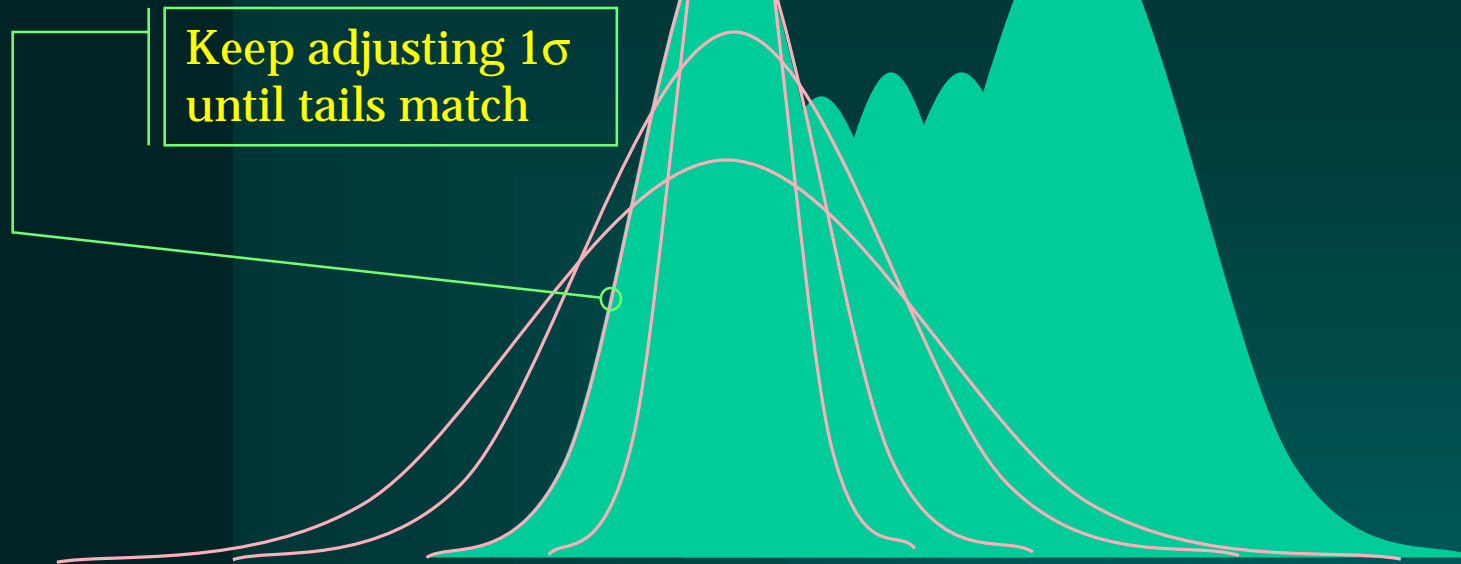
Non-Gaussian Distributions

- In order to determine the probability of a measurement occurring at the $-3\sigma_L$ point, it is critical to determine the standard deviation that would correspond to a Gaussian Distribution with a identical tail region to that of our multimodal non Gaussian distribution.
  - Note that the matched Gaussians are not necessarily the same. Either tail can exhibit a larger standard deviation

Determining Representative Gaussian Distributions

Keep adjusting 1σ
until tails match

- TailFit^{TM} algorithm enables the user to identify a Gaussian curve with a symmetrical tail region to that of the non-Gaussian distribution under evaluation.
    - Various curves are fitted against the distribution until an optimal match is found. Then, the 1σ of the matched curve is used as the standard deviation multiplier for that particular tail. This is repeated for both sides of the distribution.
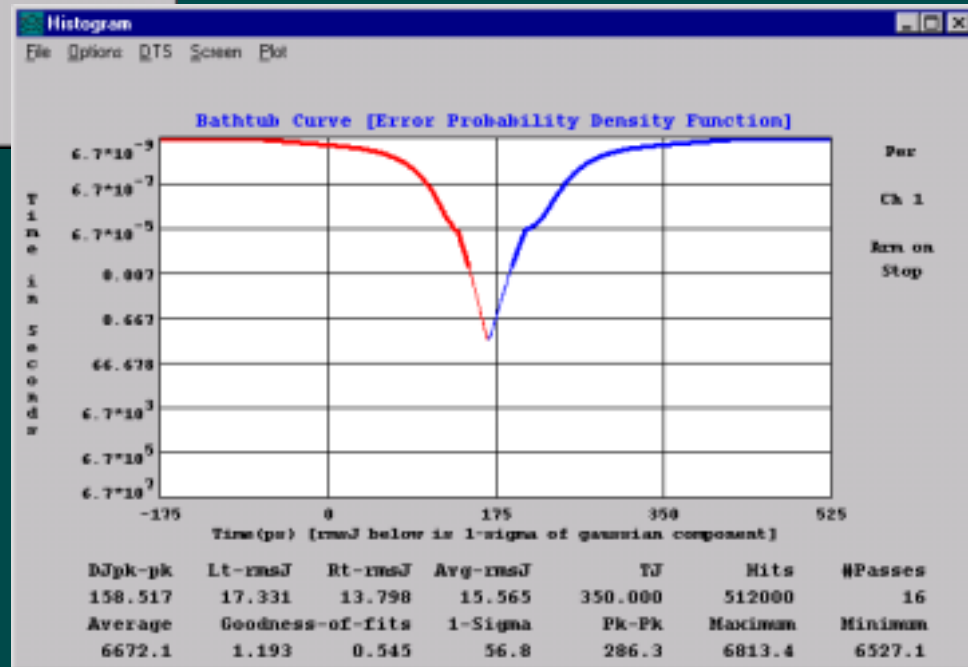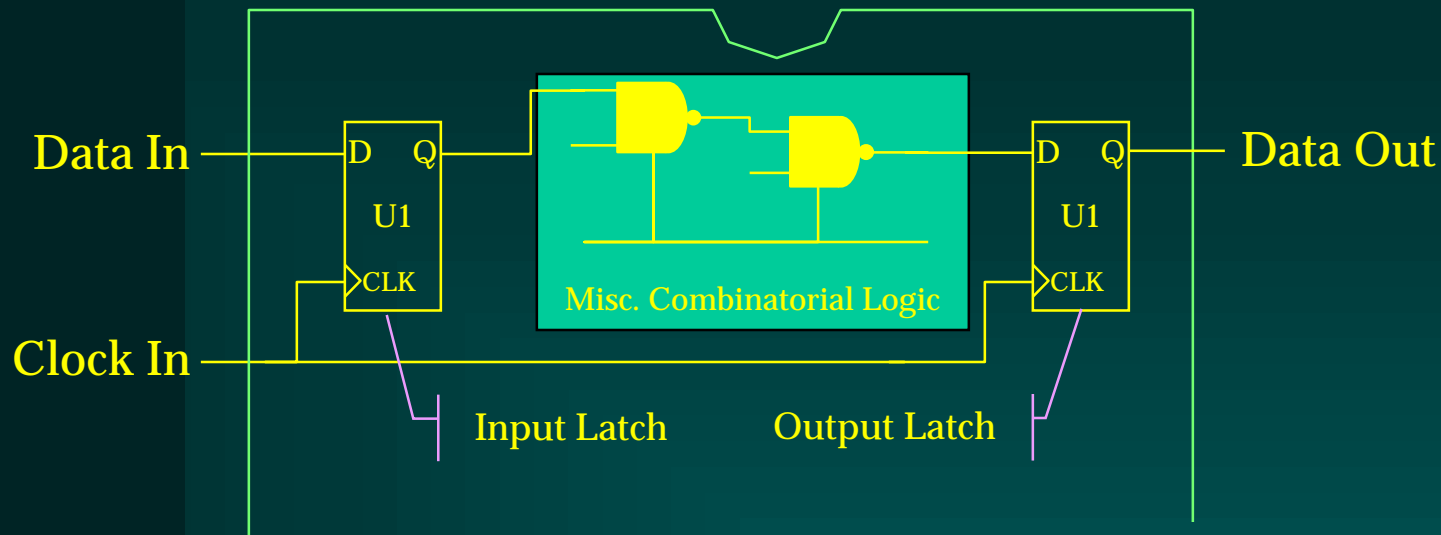
An Example of Tail Fit Technique
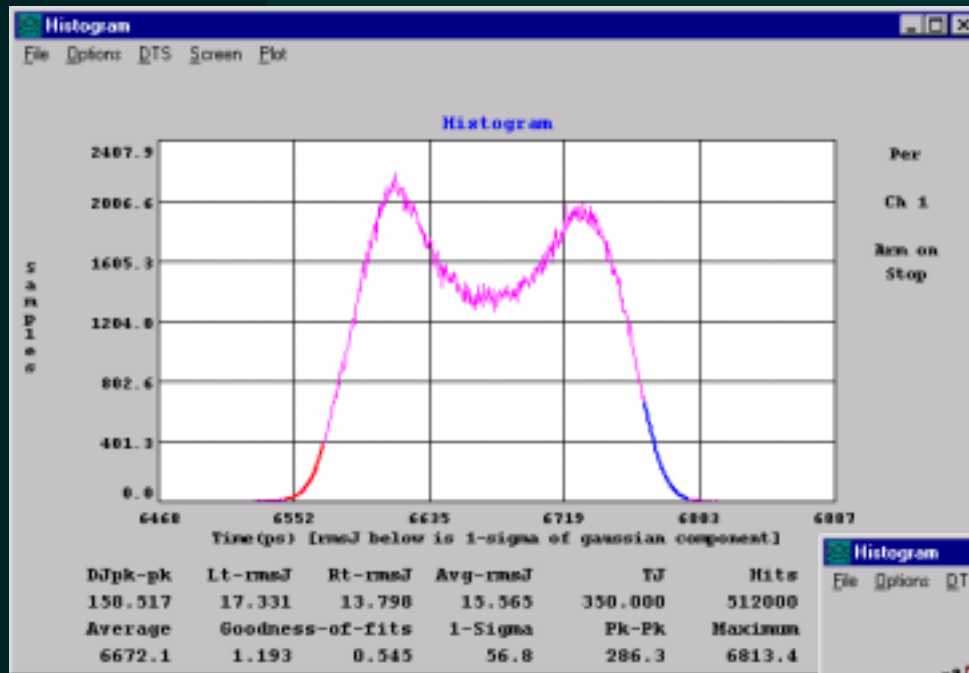
The picture to the left is an example of a distribution with both Random Jitter and Deterministic Jitter. Notice how the Tail Fit curves closely match the tail regions of the distribution.

The $1\sigma_L$ and the $1\sigma_R$ can be used to predict short cycle and long cycle probability. The plot to the left is a BER plot of period jitter vs spec. This device fails a 550ps jitter spec every 20s of operation.

Histogram

File Options DTS Screen Plot

Histogram

DJpk-pk	Lt-rmsJ	Rt-rmsJ	Avg-rmsJ	TJ	Hits
158.517	17.331	13.798	15.565	350.000	512000
Average	Goodness-of-fits	1-Sigma	Pk-Pk	Maximum	
6672.1	1.193	0.545	56.8	286.3	6813.4

Time (ps) [rmsJ below is 1-sigma of gaussian component]

Histogram

File Options DTS Screen Plot

Bathtub Curve [Error Probability Density Function]

Time (ps) [rmsJ below is 1-sigma of gaussian component]

DJpk-pk	Lt-rmsJ	Rt-rmsJ	Avg-rmsJ	TJ	Hits	#Passes
158.517	17.331	13.798	15.565	350.000	512000	16
Average	Goodness-of-fits	1-Sigma	Pk-Pk	Maximum	Minimum	
6672.1	1.193	0.545	56.8	286.3	6813.4	6527.1

How does Clock Jitter Effect Systems?

Data In — D Q — U1 — CLK — Misc. Combinatorial Logic — D Q — U1 — CLK — Data Out

Clock In

Input Latch   Output Latch

- **Typical Synchronous Device is susceptible to short cycle errors.**
  - This device would latch the wrong data into the output latch if the period was to short. Therefore, the critical measurement for this device is period jitter (rising edge to next adjacent rising edge).
  - This is a typical problem for most synchronous devices and systems.
  - This is some times referred to as "Cycle to Cycle"
    - See Appendix for Intel ® Pentium II & III spec and Tektronix application notes for further details

# Period Stability (Period Jitter)

t_{PER}

DTS 207x

CH2

CH1

μP

BCLK

Memory

BCLK

Measure as t_{PD} for combined skew and clock jitter
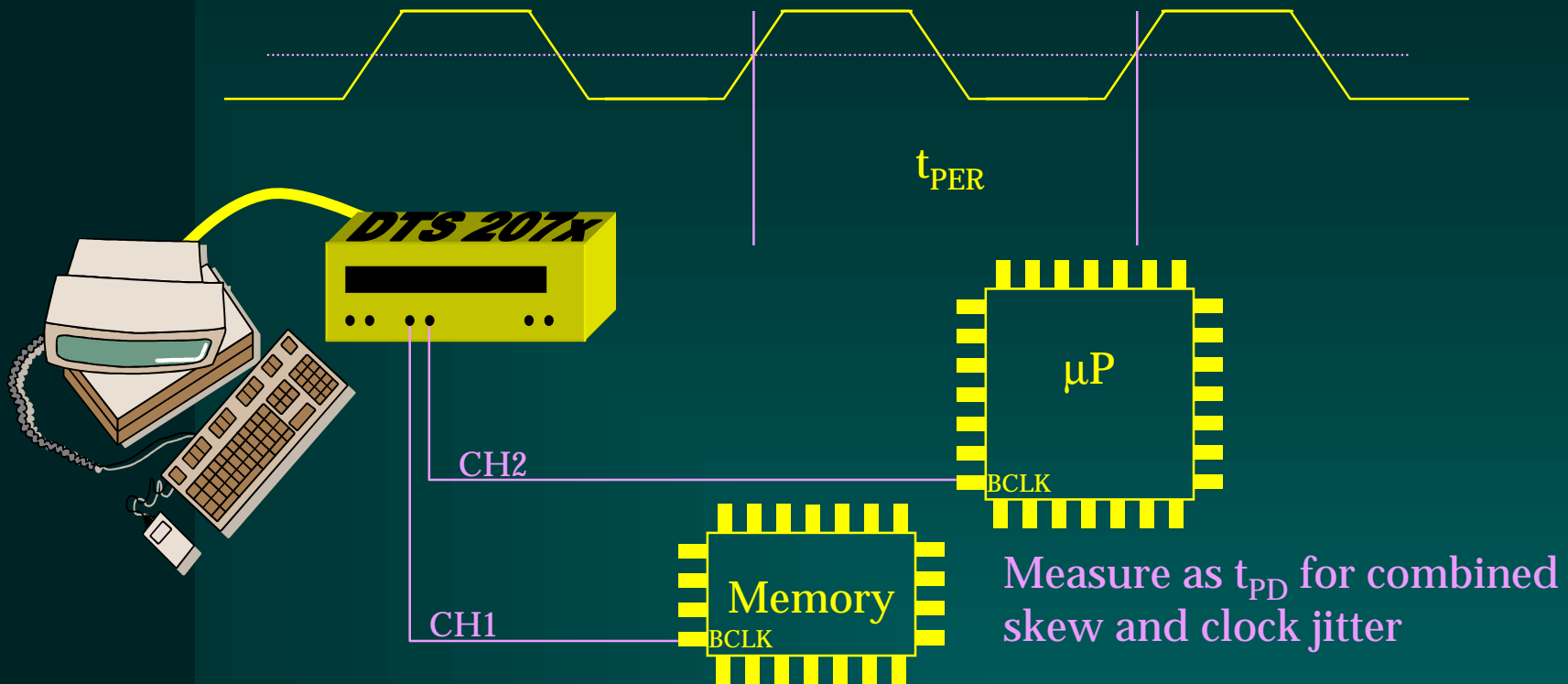
- **Intel Period Stability Specification:**

  "…should be measured on the rising edges of adjacent BLCKs crossing 1.25V at the processor core pin. The jitter present must be accounted for as a component of BCLK timing skew between devices."

  intel® Pentium® II Datasheet, pg 27

Example Debug Session
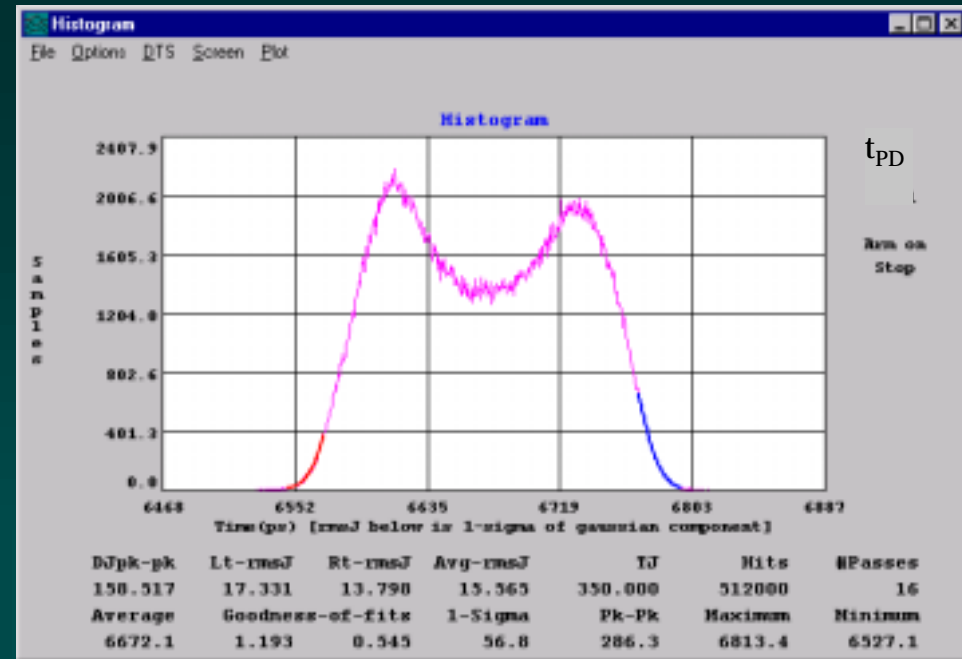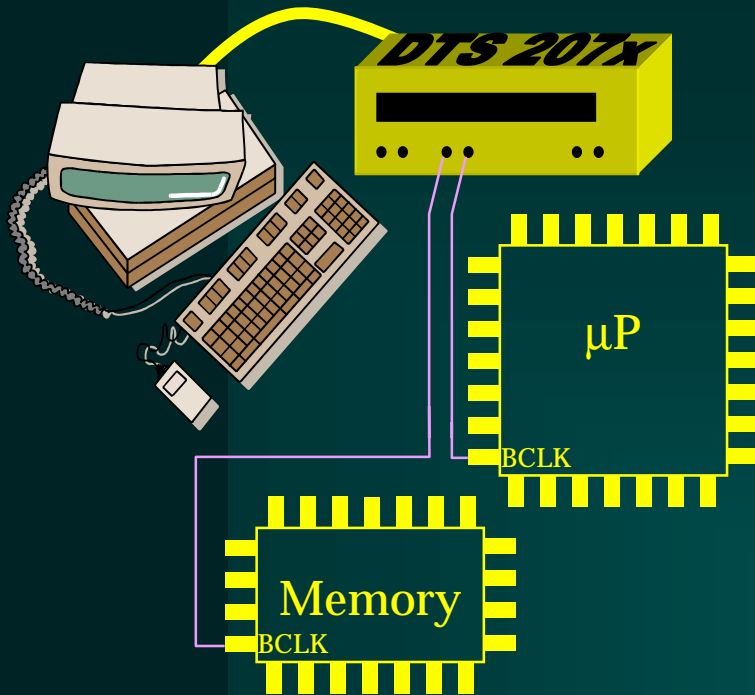
- In this example, note the presence of DJ.
  - The next step would be to determine if the DJ is due to cross talk, pattern dependency, or EMI interference.
  - Use Accumulated Time Analysis to determine Frequency of PJ
  - If PJ is a multiple frequency of clock, use Function Analysis to determine where, if at all, in the pattern the jitter is a maximum.

What is Accumulated Time Analysis^{TM}?

- ## The key to Periodic Jitter Detection.
  - Accumulated Time Analysis is a technique that uses accumulated jitter to determine the presence of periodic jitter.
  - Using ATA, the user can quickly and simply measure the cumulative amplitude and frequency of modulation for all Periodic Jitter elements riding on the clock.
  - Using a patented normalization technique, the user can also see the worst case period deviation due to each of the PJ components.

- ## What is Cumulative Jitter?
  - Periodic Jitter has the effect of increasing the period and decreasing the period of a clock over time.
    - For example, suppose a clock has a frequency of 100MHz and has a 1MHz Periodic Jitter riding on it which has a peak amplitude of 2ns.
      - The Periodic Jitter will increase the period for 50 consective periods, then, the PJ will decrease the period for 50 consecutive periods.
      - The worst case cumulative period push out occurs after the 50 increasing periods.
      - The worst case cumulative period contraction occurs after the 50 decreasing periods.
      - If the user measures the time elapsed for a random sample of 50 periods, the distribution would be bimodal, and, the time distance between the two peaks would be 2ns. Further, the worst case period push out for a single period would be less than 20ps.

The effect of a Periodic

Ideal Clock

Real Clock

Period Jitter Amplitude

Period Increasing Period Decreasing Period Increasing Period Decreasing
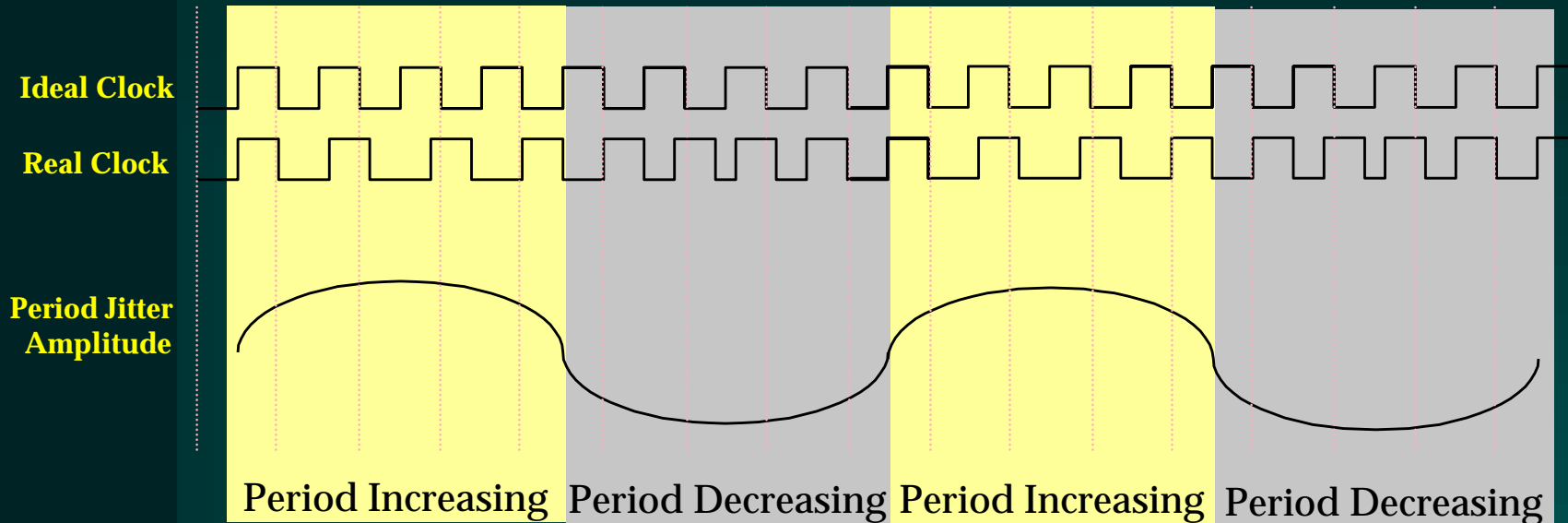
- ## Period Increasing
  - In this section the period of the modulated clock is increased from the ideal. Notice how much longer the elapsed time for 5 periods.
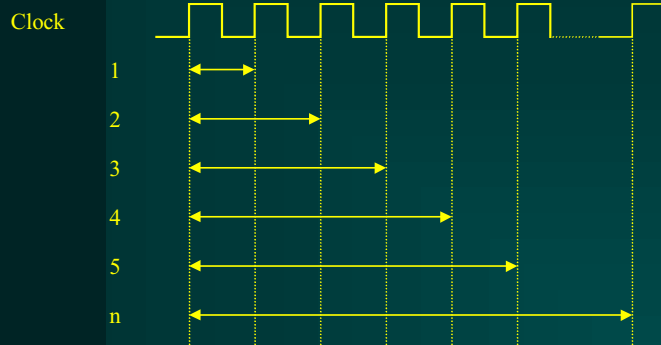
- ## Period Decreasing
  - In this section the period of the modulated clock decreases from the ideal. The net effect of the shorter periods results in a canceling out of the increased periods from the prior section. Note that the same number of clocks is completed after both sections.
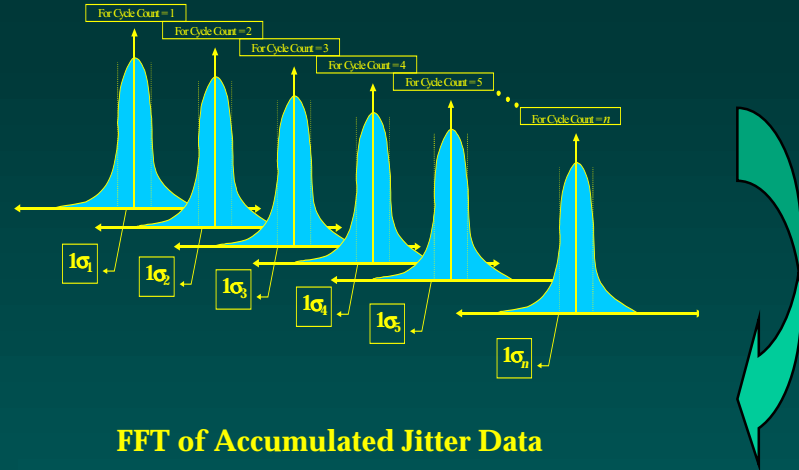
It is important to note that the sampling of the waveform must be random so as not to filter any periodic elements.
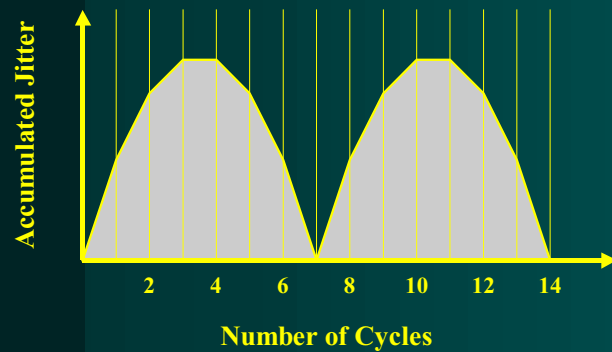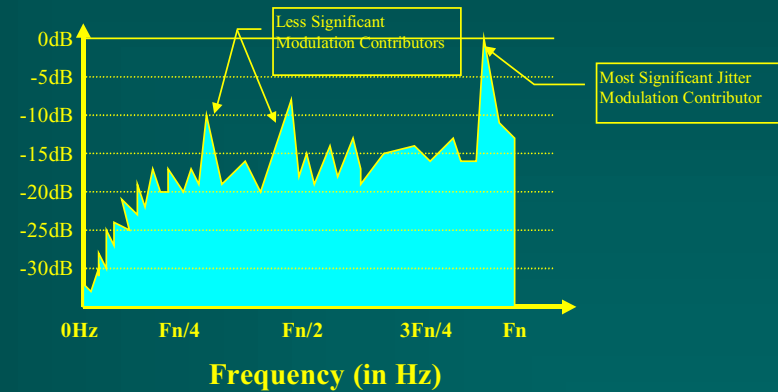
Accumulated Time Analysis™

Measurement Schedule

Distribution of Time Measurements

Clock

1

2

3

4

5

n

For Cycle Count = 1
For Cycle Count = 2
For Cycle Count = 3
For Cycle Count = 4
For Cycle Count = 5
For Cycle Count = n

$1\sigma_1$
$1\sigma_2$
$1\sigma_3$
$1\sigma_4$
$1\sigma_5$
$1\sigma_n$

Jitter Analysis Graph with Period as Function

Accumulated Jitter

2　　4　　6　　8　　10　　12　　14

Number of Cycles

FFT of Accumulated Jitter Data

Less Significant
Modulation Contributors

Most Significant Jitter
Modulation Contributor

0dB
-5dB
-10dB
-15dB
-20dB
-25dB
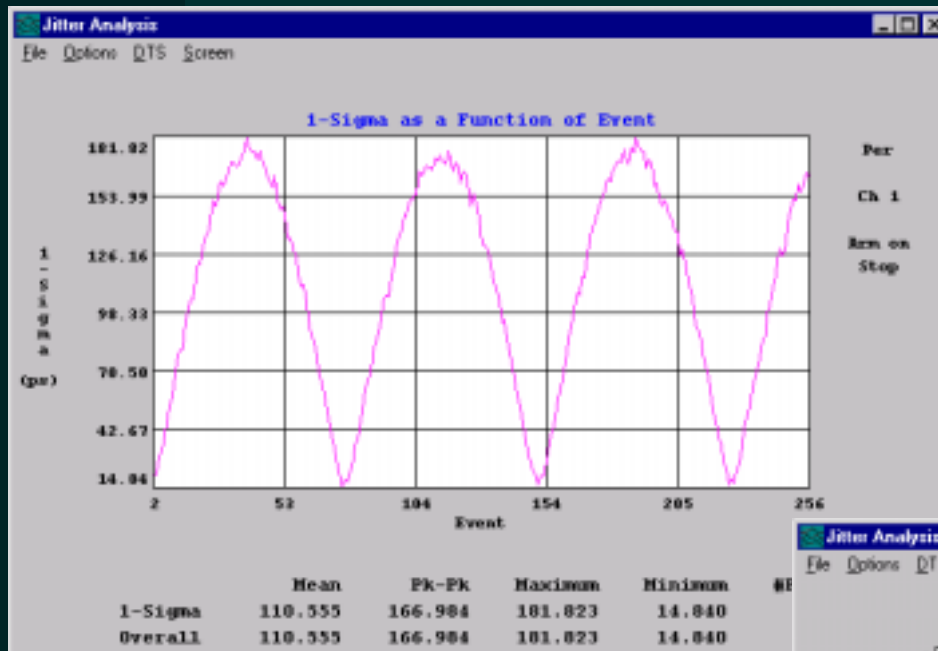-30dB

0Hz　　Fn/4　　Fn/2　　3Fn/4　　Fn

Frequency (in Hz)

*Fn = Apparent Nyquest Frequency*

Using Accumulated Time Analysis

The modulation domain plot to the left indicates a strong periodic with a cumulative jitter amplitude of 101.2ps.

The frequency domain plot to the right indicates a strong periodic at about 1MHz. This tool can also be configured to normalize the peak amplitudes of each periodic element to it's exact effect on a single period. This is called 1-clock normalization.
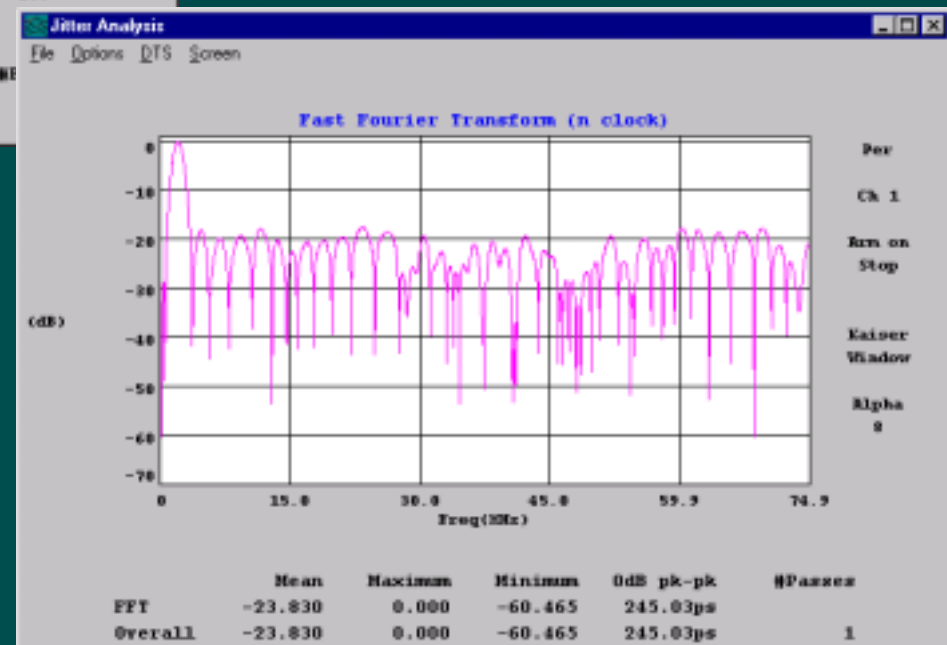
Pattern Dependant Jitter

- In some cases, the jitter on the clock could be correlated to other electronic activity near by.
  - This could be the case in an imbedded PLL application in which some other circuit in the ASIC is causing the internal PLL to jitter tremendously.
  - In the case of a system design, perhaps another part of the circuit board is emitting an excessive amount of EMI that is interfering with the operation of the PLL or is inducing modulation on the traces distributing the clock signal.

- Debug this using Function Analysis
  - The user can also debug using an oscilloscope and a pattern marker.
    - For sampling oscilloscope, make sure the stability of the reference does not exceed the DJ being diagnosed
    - For real time sampling oscilloscope, make sure the record length completely captures one execution of the pattern.
  - Wavecrest Function Analysis Tool allows the user to look at each and every period after a pattern marker to evaluate pattern dependant jitter.
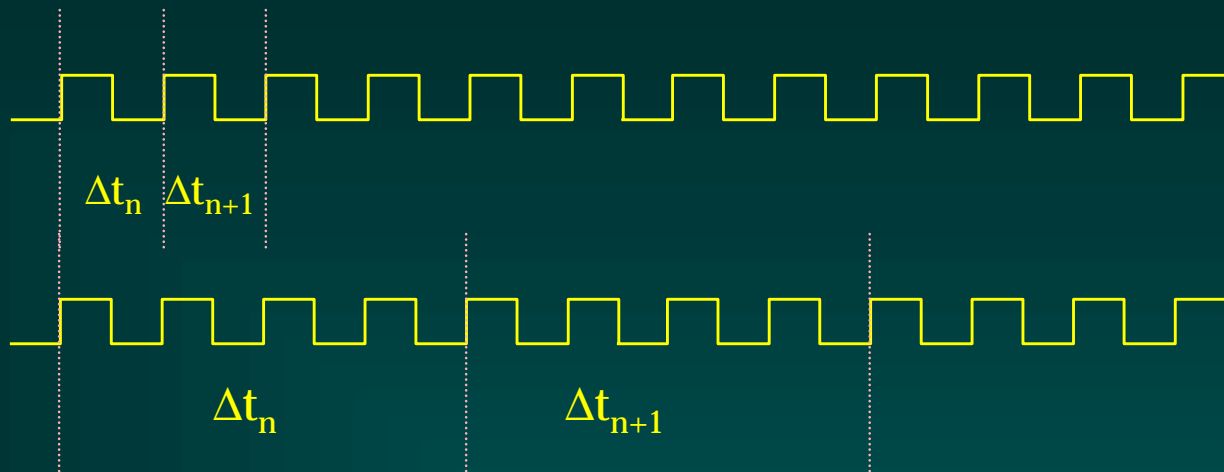
Using Function Analysis

Pattern Marker
Clock

WAVECREST   Feb 1, 2000   27
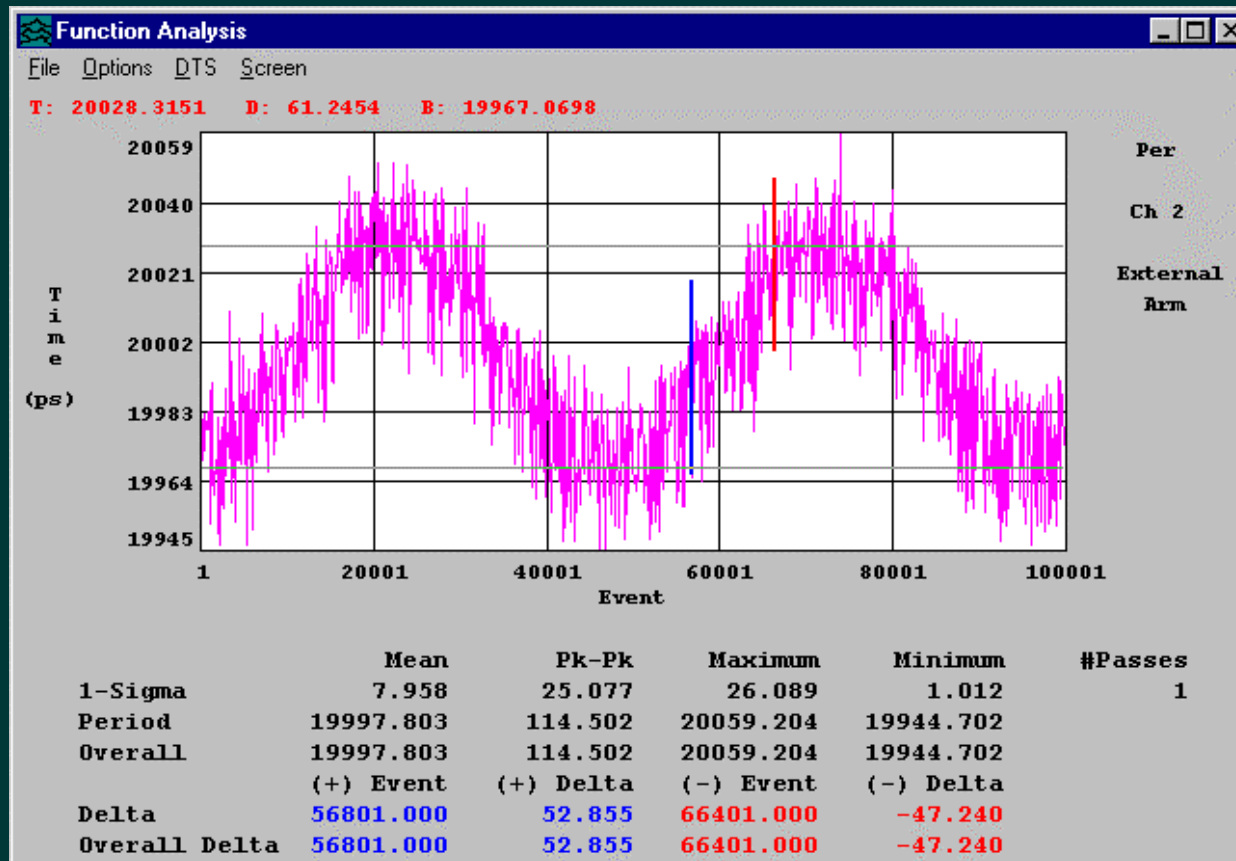
Adjacent Cycle Jitter (Rambus Jitter)

Δt_n Δt_{n+1}

Δt_n Δt_{n+1}

- ## Adjacent Cycle Jitter
  - Referred to by Rambus as "Cycle-to-Cycle"
    - Since this is inconsistent with established definitions from Tektronix, Intel, Hewlett Packard (Agilent),Wavecrest and many others, we will simply refer to this jitter phenomena as "Adjacent Cycle Jitter"
  - Adjacent Cycle Jitter is the worst case period deviation from one period to the next adjacent cycle. Measurement must be taken at exactly the same voltage for stop as well as start. Rambus requires that 10,000 adjacent periods be analyzed for compliance.

How do you measure Adjacent Cycle Jitter?

- ## Real Time Oscilloscope.

  – Jitter spec is 50 ps and rise time can be as fast as 160ps.

    - Therefore, for enough samples (3 per edge) on each rising/falling edges, use a real time oscilloscope with a sampling rate of at least 33ps. This is equivalent to a 33GHz Real Time Sampling Oscilloscope.

    - For the accuracy of 50ps, try to get a real time sampling oscilloscope with at least 10x the noise floor and 10x the resolution. So, the ideal real time oscilloscope should have a sampling rate of at least 200GHz.

    - Anything less is a coarse estimate.

- ## Wavecrest DTS.

  – Wavecrest DTS does not directly measure Adjacent Cycle Jitter.

    - Random Jitter is the overwhelming contributor to worst case Adjacent Cycle Jitter. Deterministic Jitter is a small contributor.

  – Using TailFit^{TM} to estimate TJ for a 3σ reliability is the most accurate way of estimating worst case adjacent cycle jitter over 10,000 adjacent clocks.

    - Deterministic component will automatically be normalized to single period.

    - Random Jitter will be calculated for 10,000 adjacent clocks.

    - Random Jitter and Deterministic Jitter will be combined to form worst case adjacent cycle jitter estimate for the desired 10,000 adjacent periods.

    - Measurement can be made for any number of cumulative periods.
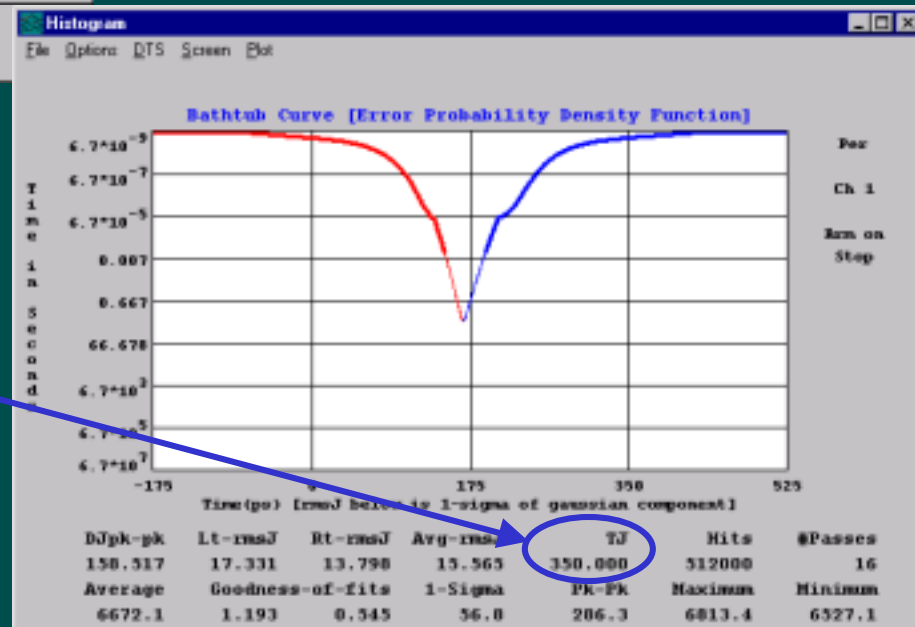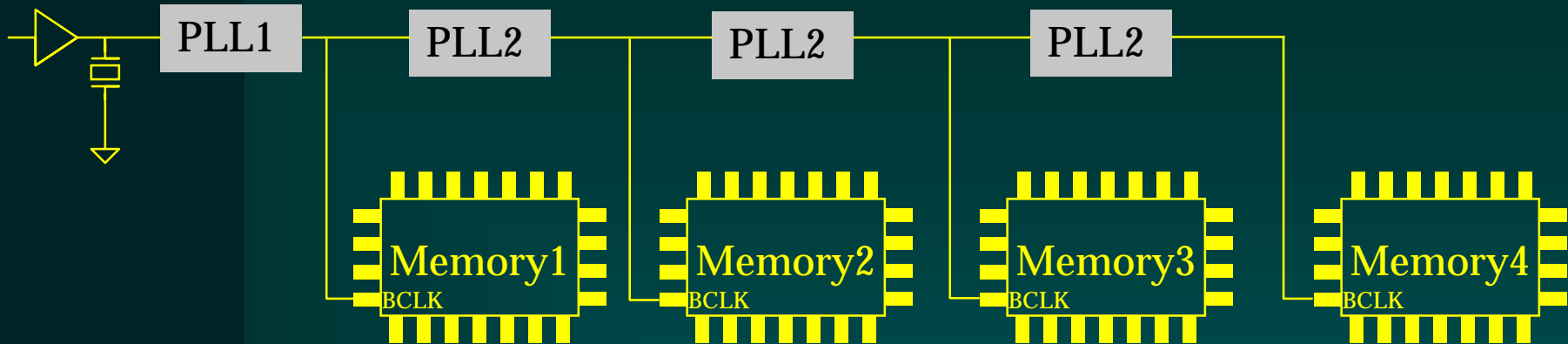
Measuring Adjacent Cycle Jitter
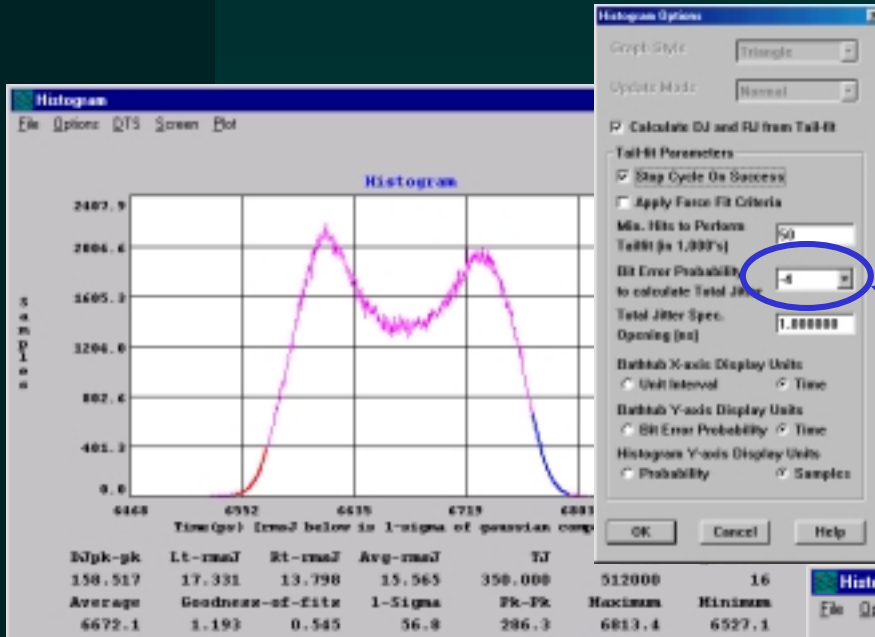
Set Bit Error Probability to (-4) for TJ estimate of 10,000 cycles.

Watch real time effects on TJ while changing other ambient conditions.
Also, note jitter contributors.
Is jitter from DJ, RJ_L or RJ_R?

What Happens to Downstream Devices?

PLL1 — PLL2 — PLL2 — PLL2

Memory1 BCLK   Memory2 BCLK   Memory3 BCLK   Memory4 BCLK

- **PLL Bandwidth**
  - All PLL devices have a cutoff frequency which defines the maximum modulation frequency that PLL can track. Modulation frequencies above the cutoff frequency are simply ignored.
    - So, if EMI radiation of 2MHz were induced after PLL1, and PLL2 has a cutoff frequency of 500kHz, then, Memory 1 will see the modulation on it's clock input while Memory 2 will not.
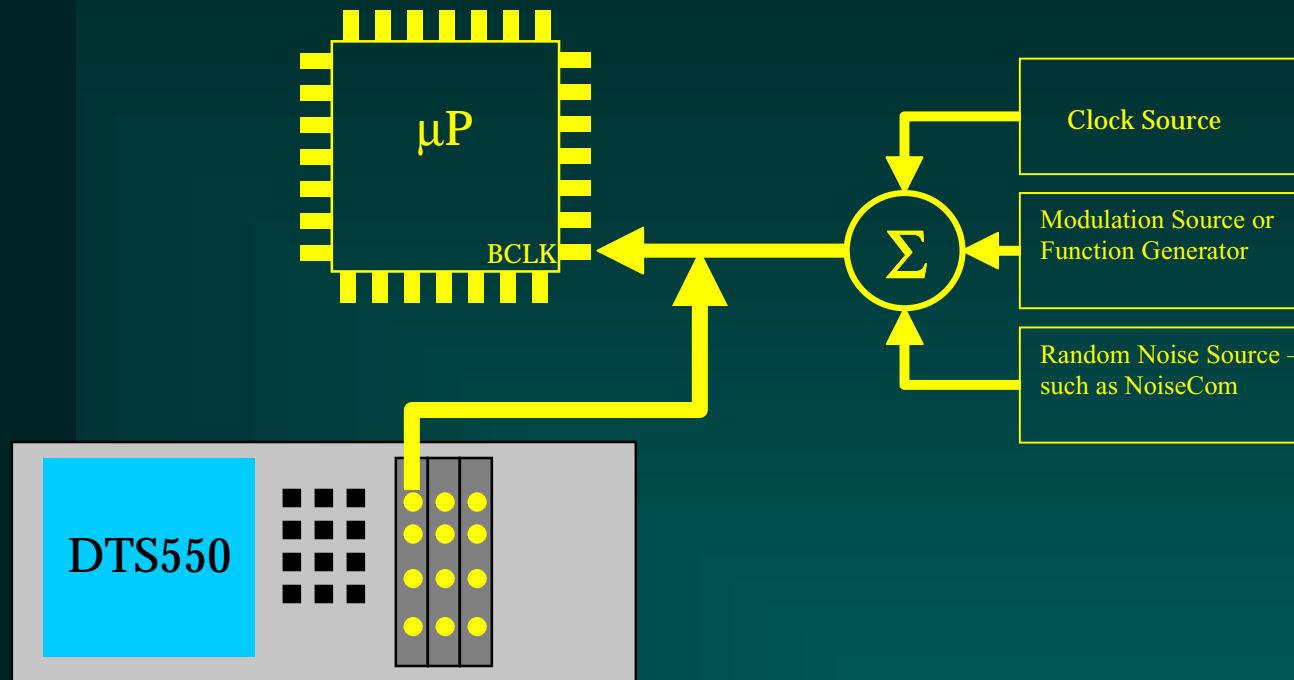
  (Watch for future Wavecrest tools to measure PLL Bandwidth, loop response, dampening coefficient and much, much more.)

- **Jitter Tolerance**
  - The downstream devices may be susceptible to many forms of jitter caused by the circuit design, ambient environment or even the PLL driving it. Jitter Tolerance is a measure of how much Jitter a device can handle and still function properly.

Jitter Tolerance In a Digital Network

μP

BCLK

Σ

Clock Source

Modulation Source or Function Generator

Random Noise Source – such as NoiseCom

DTS550

- Substitute Jitter Generator for PLL signal at each device to test maximum allowable jitter.
  - Can use a series of instruments including a clock source, modulation source and Random Noise Source.
  - Can also use Wavecrest DTS550 Jitter Generator for up to 1GHz clock emulation with full jitter programmability.

- Sweep through frequency range for modulation sensitivity testing.
  - Many internal circuits feature an embedded PLL
  - Since all PLL devices have a bandwidth, it is important to sweep the modulation frequency through several different frequencies to determine specific sensitivities.

- Use several different Jitter combinations.
  - Increase psuedo random jitter to test for Random Jitter,
  - Sweep Periodic Jitter through several frequencies and amplitudes.
  - Check Power sensitivities to jitter tolerance.
  - Check thermal sensitivities to jitter tolerance.