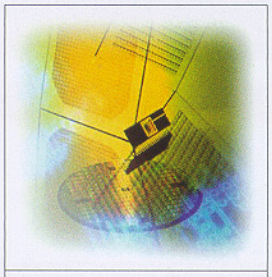
Wavecrest has recently announced a new technique to analyse jitter to FC-MJS specifications (bit error rate (BER) of 1e-12) on optical interfaces without the need for extracting a clock from the serial data stream. The technique is ideal when 'normal traffic' is being run and test patterns are not possible.



TEST & MEASUREMENT

Assuring the signal integrity of the Internet infrastructure through jitter analysis

Dennis Petrich ■ Wavecrest Corporation

Until now, analysis of optical/electrical data communications interfaces running random traffic for storage area networks, disk drives, hubs, switches, routers and retimers at the module, board and system level has been limited to eye diagrams. The drawback of these is that they do not measure BER or total jitter (TJ) of all traffic to NCITS specifications.

The technical breakthrough came with the development of a workable TailFit™ algorithm (patent pending), to separate deterministic and Gaussian jitter components from the timing distribution. With this information an equivalent BER can be calculated using the documented FC-MJS algorithms. The advantage of this DSP approach is speed and ease of use and correlation because no clock extraction is required.

The DSP approach also applies the first-order PLL model to the results to simulate the effects of an extracted clock. By applying a model instead of using a real recovered clock, variations in recovered clock hardware are eliminated from the measured results, making correlation to specifications much simpler.

Additionally, eliminating the PLL hardware removes the frequency dependency the equipment has on data rate and makes this new DSP technique data-rate agile and usable for any protocol to the high-frequency limit of the equipment. Fibre Channel, Ethernet, Gigabit Ethernet, SONET, ATM and 1394B can all be tested with the same hardware.

The new method

The newly developed method uses the above-mentioned DSP technique to calculate the total jitter number at a BER of 1e-12 in a fraction of the time it takes the BERT running tests under ideal conditions. This new technique also shows the jitter power spectral density and gives the user insight into potential jitter sources if compliance is not met – information the BERT is not able to provide.

All of the analysis is carried out on the optical/electrical serial data signal requiring no other connections to any other signals – making correlation more easily repeatable. This technique has been correlated to the BERT under ideal conditions to show correlation between the FC-MJS and BERT solutions. The FC-MJS equivalent methodology was originally developed as a technique to speedup BER testing and to eliminate the need for a bit clock, but, until the development of a workable TailFit algorithm, was only usable under ideal conditions and not under real traffic conditions as is now possible.

Figures 1 and 2 show correlation to the BERT with a normal running series of 'Idle' characters and a 'PRBS 2e7-1' pattern. Three techniques are being correlated to the BERT in these two figures. The correlation was carried out using the Wavecrest DTS in three of its test modes – using a pattern marker, a reference bit clock and no clock/no marker. The results show close correlation of the equivalent total jitter to the actual total jitter measured by the HP 71600B BERT using the reference bit clock. ●

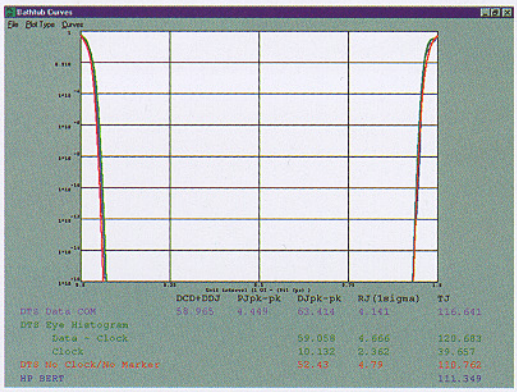


Figure 1. Bit Error Rate Probability Curve for the 'Idle' character pattern.

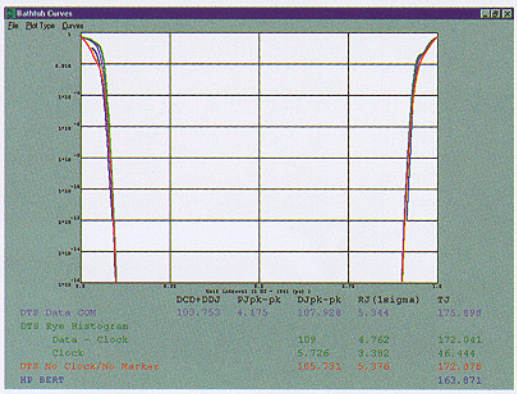


Figure 2. Bit Error Rate Probability Curve for the 'PRBS 2e7-1' pattern.

BIOGRAPHY

Dennis Petrich has been working in the field of test and measurement technology for the past 29 years. He holds five patents relating to time-measurement techniques with four more patents pending based on current jitter analysis research. Mr Petrich is the original inventor of the Delay Lock Loop (DLL) used today in many clock de-skewing circuits.

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