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# Transfer Functions For The Reference Clock Jitter In A Serial Link: Theory And Applications in PCI Express

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# Abstract

Transfer functions for the reference clock jitter in a serial link such as the PCI Express 100 MHz reference clock are established for various clock and data recovery circuits (CDRCs). In addition, mathematical interrelationships between phase, period, and cycle-to-cycle jitter are established and phase jitter is used with the jitter transfer function. Numerical simulations are carried out for these transfer functions. Relevant eye-closure/total jitter at a certain bit error rate (BER) level for the receiver is estimated by applying these jitter transfer functions to the measured phase jitter of the reference clock over a range of transfer function parameters. Implications of this new development to serial link reference clock testing and specification formulation are discussed.


# Author Biography

## Mike Li

Dr. Mike Li is currently the Chief Technology Officer (CTO) with Wavecrest. Dr. Li pioneered jitter separation method (Tailfit) and DJ, RJ, and TJ concept and theory formation. He has involved in setting and contributed to standards for jitter, noise, and signal integrity for leading serial data communications, such as Fibre Channel, Gigabit Ethernet, Serial ATA, and PCI Express. Currently he is Co-Chairman for PCI Express jitter standard committee. Dr. Li is sitting on the technical committees for IEEE and IEC sponsored technical conferences such as International Test Conference (ITC) and Designcon and is a constant speaker, invited speaker, panelist, session and panel chairs on the subjects of jitter/noise and signal integrity.

Dr. Li has more than 10 years experiences in high-speed related measurement instrumentation, testing, and analysis/modeling algorithms/tools, with applications in IC, microprocessor, clock, serial data communications for both electrical and optical, and wireless communication. Prior joining Wavecrest, Dr. Li had worked in both industry and academic institution. He has a BS in physics from University of Science and Technology of China, a MSE in electrical engineering and a Ph.D. in physics from University of Alabama in Huntsville. He did his Post Dr. at University of California, Berkeley and worked there as a research scientist on high-energy astrophysics before he joined industry. Dr Li has published more than 40 papers in refereed technical journals, holds 2 patent and has 7 patents pending.

## Andy Martwick

Mr. Martwick is a circuit architect at Intel Corporation’s chipset division. He authored sections of the 3GIO physical layer specification and co-chairs the PCI Express jitter workgroup. He has over 20 years of product and design experience, and over 25 patents in computer architecture and communications.

## Gerry Talbot

Gerry Talbot is a Senior Follow at AMD, his primary focus is high-speed IO design, involving the development of, and contributing to, industry standard specifications such as HyperTransport, PCI Express, PCI266/533 and FB-DIMM. His work involves silicon circuit design, system level jitter modeling, interconnect channel modeling and signal integrity simulation.

## Jan Wilstrup

Mr. Wilstrup is a corporate consultant at Teradyne Inc. His present interests are SI simulation and analysis, signal and noise analysis methods and analog circuits. He holds 4 patents and has 7 patents pending in the instrumentation area. He studied mathematics and physics at the University of Minnesota.

# 1.) Introduction

The serial data communication architecture has been proven to have the capability of carrying data over fiber medium at a rate > 100 Gb/s. The architectures of these serial communication links are characterized by the fact that the bit clock is embedded in the transmitted bit stream and it is recovered by a clock recovery (CR) function at the receiver side of the link. Typically the CR is implemented by using a phase-locked loop (PLL). Figure 1 shows a basic block diagram for a simple serial link and related clock recovery function.

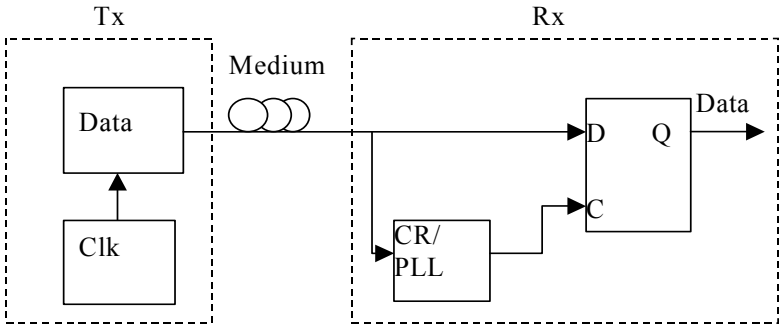


Figure 1. A schematic block diagram for a serial communication

Meanwhile, personal computer (PC) and main-frame work station communication links and I/O buses have also evolved from a parallel bus where a synchronized global clock is distributed with each data path, to source synchronized I/O where the data is strobed by the clock at the receiver register, to serial data I/O similar to those network I/O architectures. At data rates > 1 Gb/s, most of the communication links converge to serial architecture with embedded clock or reference clock, plus a clock recovery function. Typical network centric network standards include: Fibre Channel (FC) and Giga Bit Ethernet (GBE); and typical PC I/O standards at > 1 Gb/s are PCI express (2.5 Gb/s for generation I) and Serial ATA (1.5 Gb/s for generation I).

The key performance merit for a serial communication link is the BER. The root causes for non-zero BER are timing jitter and amplitude noise. However, since BER is a system performance merit, the system transfer functions for jitter and noise must be incorporated into the equation to quantify it. A simple generic receiver jitter transfer function model has been established [1][2] based on the receiver architecture as shown in Figure 1. The schematic diagram of such model is shown in Figure 2.

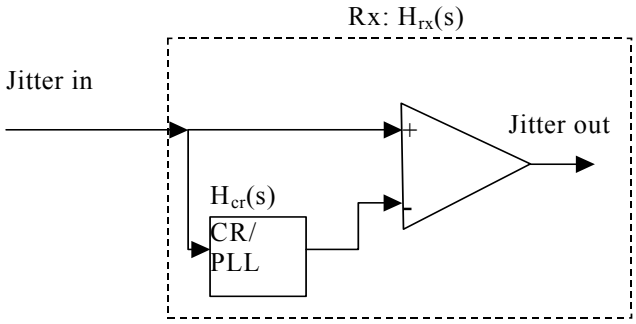


Figure 2 A schematic diagram showing that the receiver jitter transfer is the difference function between the data and clock inputs to the receiver data retiming logic.

The essence of this model is that the jitter transfer function is the "difference" between the data signal and the recovered clock signal. In the context of Figure 2, such a transfer function can be represented by: $H_{rx}(s) = 1-H_{cr}(s)$, where $H_{rx}(s)$ is the jitter transfer function for the receiver, $H_{cr}(s)$ is the frequency transfer function for the clock recovery, and s is the complex frequency. Most clock recovery circuits have a low-pass characteristic, such as PLL-based clock recovery circuits. Since $H_{cr}(s)$ is low-pass, therefore $H_{rx}(s)$ will be high-pass due to the difference function, resulting low-frequency jitter being tracked or attenuated by the receiver. Receiver architectures for network I/O links, such as FC and GBE, all have high-pass jitter transfer functions. A BER of $10^{-12}$ or less is a commonly accepted maximum value for most communication standards.

While both network and PC serial communication standards share some similarities at rates > 1 Gb/s: they both use asynchronous serial data transfer schemes and clock recovery at the receivers. However, there are some significant differences. For example, network communication link components are typically low-volume and high-cost, and this gives the designer the luxury to use relatively expensive, high-quality, and low-jitter components, such as an oscillator or a clock generator. In contrast, PC communication link components are typically high-volume and low-cost, preventing the designer of using high-cost and low-noise components, such as a low-jitter clock source; yet, the system still needs to maintain a similar BER performance as the network I/O link. This is the major challenge for designing a PC I/O link, such as PCI Express. One key difference in PC serial I/O links is the CR function of the receiver. In PC serial applications the CR may be implemented using low-cost digital methods such as a phase interpolation (PI)[4] that operates differently from a conventional PLL CR. Furthermore, PC I/O links need to deal with the spread spectrum clock (SSC) that is not used for a network I/O links. SSC may degrade the BER. Considering these differences, network serial I/O architecture *cannot* be directly adopted for PC use, and some changes are needed for PC I/O needs. PC I/O links represent a new jitter and noise estimation and analysis problems, and methods need to be created for PC I/O links. Some of the established fundamental jitter models such as the "difference function" are still valid as the basis. In this paper, we will only focus on serial link reference clock jitter and use the PCI Express I/O link[3] as a benchmark.

Even though we only focus on PCI Express, it is not realistic to address all the jitter and noise challenges in a single paper such as this one due to their complexity. We will only focus on the system jitter transfer function for the 100 MHz reference clock jitter. Our goal is to establish an appropriate relevant jitter definition and jitter transfer function so that the total eye-closure (or total jitter) at a certain BER can be estimated at the receiver side, given the reference clock jitter. We will discuss various jitter definitions and their interrelationships in section 2 and select the appropriate one to work the system jitter transfer function. In section 3, we will develop the system jitter transfer functions based on PCI Express I/O link system architecture, for clock and data recover schemes that use a PI or a PLL. Corresponding numerical simulations for the transfer functions and their dependences on the model parameters were also carried out. In section 4, we apply the developed transfer function to some measured reference clock phase jitter and study how will it be changed by the transfer functions and estimate the worst case eye-closure at the receiver with the transfer function parameters. In section 5, we will give a summary and some conclusions, as well as discussion of the topics that are not covered by current paper, but will be in future publications.

## 2.) Phase, Period, and Cycle-to-Cycle Jitter and Their Inter-relationships

Various jitter definitions have been proposed for 101010 clock-like signals. Examples include time-domain cycle-to-cycle jitter and frequency-domain phase noise. However, there is no publication so far that discusses the mathematical implications for each definition and the inter-relationships between them. In order to select the appropriate jitter definition for PC serial I/O links, we need to treat those various jitter definitions in a same and coherent theory frame so that the interrelationship can be established, and persistent and interchangeable results can be obtained. We will start with the threshold crossing timing definition first.

### 2.1) Timestamps of Threshold Crossings

Assuming the data consists of a repeating 101010…. clock pattern, the measurement of each consecutive threshold crossing can be recorded and stored as an array. This is the timestamp array of the threshold crossings.

The time stamp array of the threshold crossings are equivalent to the accumulated phase of the data UI, also known as the absolute phase. In the case of the 400 ps UI for PCI Express data stream, every 400 ps then represents one complete "cycle" or "revolution" and is equal to 2π radians. The absolute phase, starts at 0 and proceeds to grow unbounded, at the rate of

$$\Theta_n \propto nT, \quad n = 0,1,2...,N \tag{2.1}$$

For the ideal case where there is no phase jitter, the first UI starts at 0 radians and ends at 2π radians. The second UI starts at 2 π radians and ends at 4π radians. The third UI starts at 4π radians and ends at 6π, and so on. Thus every UI can be thought of as one complete cycle or a complete "revolution" of the clock. T can be replaced by 2π to get the equivalent "radians" from a UI period as in

$$\Theta_n = 2n\pi, \quad n = 0,1,2...,N \tag{2.2}$$

This is shown in Figure 3, where the straight line is a measurement and the threshold crossings are exactly 400 ps apart. The stem lines have a sinusoidal error term added to them. The Y axis is the absolute phase of the signals and is represented in ns and parenthetically in radians. The X axis is the ideal clock for each measurement and is given in ns.

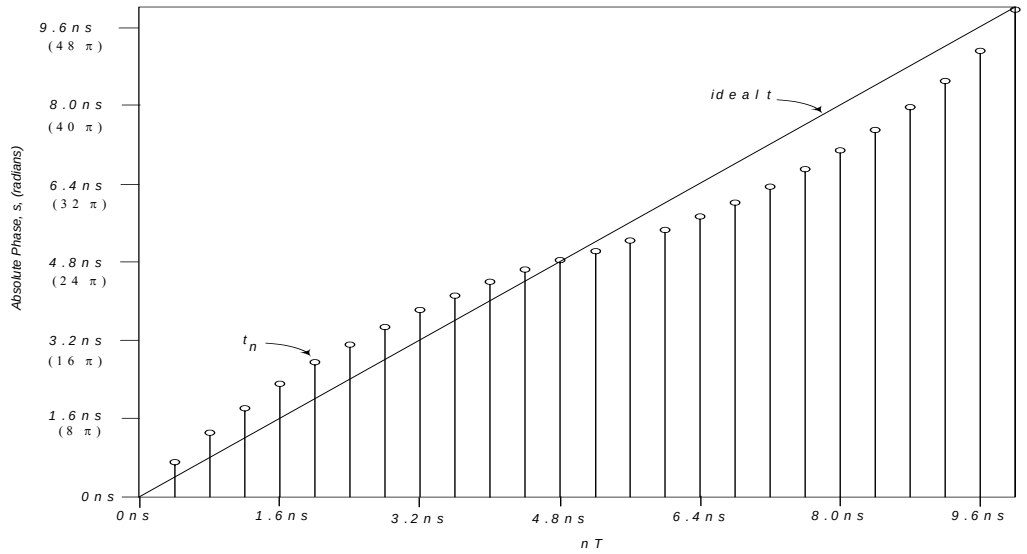


Figure 3 : Absolute phase versus nT

## 2.2) Bit Period (T) and Unit Interval (UI)

The Unit Interval is defined as the difference in a measurement and the previous measurement.

$$UI_m = t_m - t_{m-1}, \quad \mathrm{m} = 1,2,...,\mathrm{N} \tag{2.3}$$

The ideal bit period, T, is a mathematical convenience for developing the understanding of what jitter is and how to derive it. In practice, the bit period is extracted from the data itself. This extraction process produces the "recovered clock" that has the "recovered period", and is actually used in the calculations.

## 2.3) Phase Jitter (Φ)

The phase jitter is defined as the difference between the measured time and the ideal bit period T. Phase jitter is an accumulation of the time error from the ideal time of n*T.

$$\Phi_n = t_n - nT, \quad \mathrm{n} = 0,1,...,\mathrm{N} \tag{2.4}$$

Figure 4 shows an example of sinusoidal phase jitter at 100 MHz with an arbitrary magnitude of ± 450 ps shown on the Y axis.

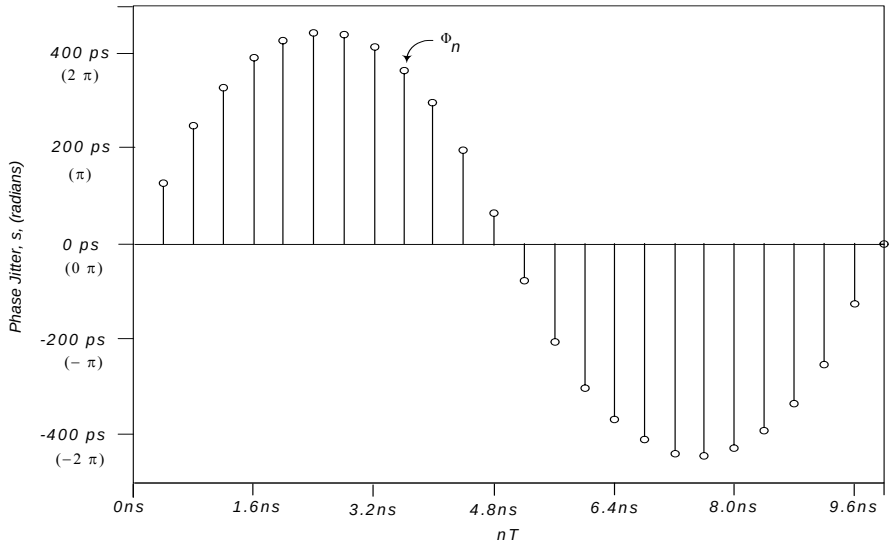


Figure 4: Phase jitter versus nT

## 2.4) Period Jitter (Φ')

The period Jitter (Φ') is the difference between the measured period and the ideal period and is defined as:

$$\Phi'_n = (t_n - t_{n-1}) - T, \quad \mathrm{n} = 1,2,...,\mathrm{N} \tag{2.5}$$

Combining equations (2.4) and (2.5), it can be shown that the period jitter, Φ', is also

$$\Phi'_n = \Phi_n - \Phi_{n-1} \quad \textbf{(2.6)}$$

This is the first difference function of the phase jitter : Φ.

Period jitter, Φ', is shown in Figure 5, where T is the ideal 400 ps. The Y axis shows the magnitude of the period jitter in ps and, parenthetically, in radians.

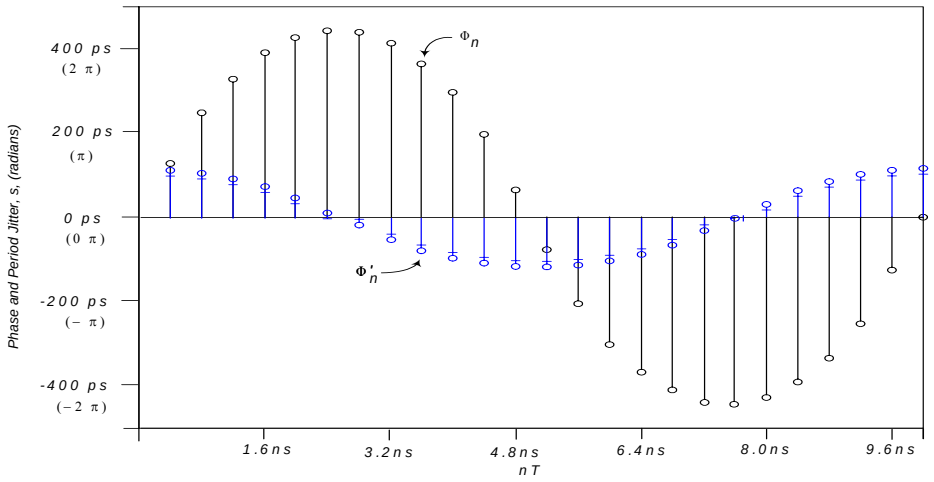


Figure 5: Phase and period jitter versus nT

## 2.5) Cycle-to-Cycle Jitter (Φ")

The cycle-to-cycle jitter is the difference between consecutive bit periods and is defined as:

$$\Phi''_n = (t_n - t_{n-1}) - (t_{n-1} - t_{n-2}), \quad n = 2,3,...,N \quad \textbf{(2.7)}$$

Combining equations (2.5) and (2.7) it can be shown that this is also

$$\Phi''_n = \Phi'_n - \Phi'_{n-1}, \quad n = 2,3,\ldots,N \quad \textbf{(2.8)}$$

and is the first difference function of Φ', or the second difference function of Φ. This is shown in Figure 6. The Y axis shows the magnitude of the cycle-to-cycle jitter in ps and parenthetically in radians.

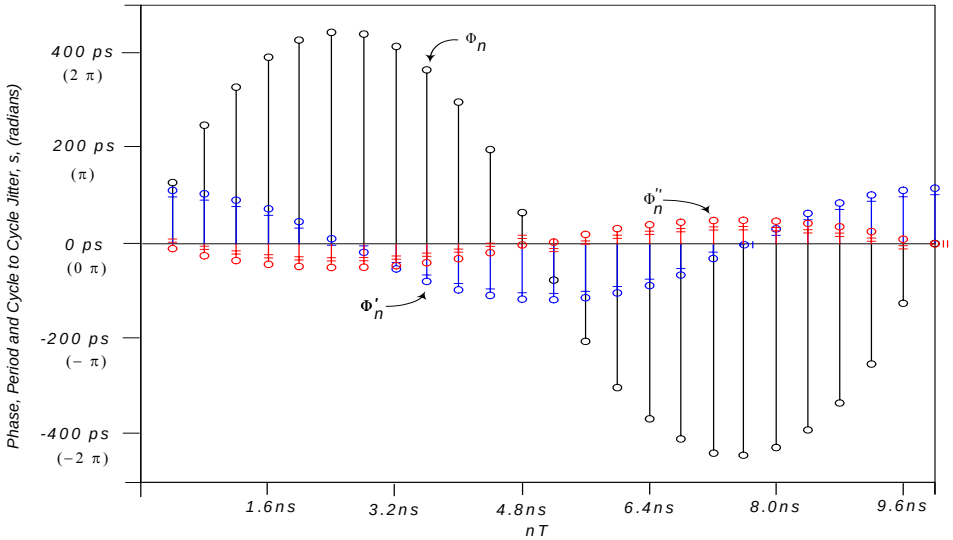


Figure 6: Cycle-to-cycle jitter and difference function of period jitter versus nT

## 2.6) Jitter Relationships

All three jitter types are shown in Figure 6 for a phase jitter magnitude of 450 ps (2.25 π radians) at a frequency of 100 MHz. The first and second difference function from Φ to Φ' to Φ'', respectively, can be seen in Figure 6.

It follows that all three designations of jitter: phase jitter, $\Phi$, period jitter, $\Phi'$, and cycle-to-cycle jitter, $\Phi''$, are different ways to represent the *same* physical behavior of the clock jitter. Given a complete record in time of jitter in any one of the forms, the other two can be derived.

Without a complete record in time, conversion between the different representations of jitter is not possible. For example, if only a peak-to-peak value for the period jitter is known then determining the peak-to-peak value of phase jitter or the peak-to-peak value of the cycle-to-cycle jitter is not possible.

An analogy can be drawn with rotational motion:

Phase jitter can be considered the relative distance that the actual (measured) phase has moved from the absolute phase of the ideal clock. In other words, it is the number of radians that the phase of the clock is vs where it should be.

Period jitter is the speed at which the phase is changing.

Cycle-to-cycle jitter is the acceleration of the phase from or to the ideal phase.

In all receiver architectures, the goal of the clock recovery is to align the sampling clock to the incoming data stream. Certain data recovery architectures, such as PI type, rely on the phase of the reference clock to grossly align the sample clocks, and then have other mechanisms to provide fine adjustment of the reference clock phase to the incoming data phase as discussed in[4]. For these types, the presence of phase jitter and the response of the components to phase jitter are critical for the proper operation of the system.

# 3.) Jitter Transfer Function Derivation and Simulations

In this section, we will first review the various clock and data recovery circuits (CDRCs) used in PCI Express I/O link. We will then establish the jitter transfer functions from the reference clock the receiver based on various CDRC topologies. Once the transfer function is obtained, we will perform the numerical simulations and reveal the characteristics of the transfer functions and its dependency on key parameters of the circuits. We then apply the transfer function to the measured jitter from the 100 MHz reference clock to estimate the relevant total jitter (or eye-closure) at the receiver. For a given BER level, the eye-closure and total jitter is related by: eye-closure (BER) = UI – TJ (BER).

## 3.1) Clock and Data Recovery Circuits (CDRCs)

We will consider three types of CDRCs for the PCI Express I/O link, the PI, the Oversampler, and PLL. The data recovery operation requires looking at the incoming data and recovering the phase and frequency of the incoming data stream, after accounting for missing threshold crossings. A clock is generated locally or through the clock recovery that matches the data phase and frequency of the incoming data and is used to sample the data at the receiver.

### 3.1.1) Digital Based

The PI and Oversampling CDRCs use a digital mechanism to achieve phase alignment of the clock with the data. They belong to the class of digital CDRCs and are not easily modeled. They also have limited ability to track changes in frequency, and, in general, rely on the systems common reference clock system and internal reference PLLs to recover the frequency information. Digital based CDRCs are known to have lower silicon cost and power consumption.

### 3.1.2) PLL Based

The PLL based CDRC does not use the common reference clock to recover the phase or the frequency. It looks exclusively at the incoming data and adjusts phase and frequency accordingly. This clock recovery scheme is widely used in network communication link and it has a well-known transfer function and the order of the transfer function can be $2^{nd}$ order or higher, providing better jitter rejection/tolerance compared with a first-order CDRC transfer function.

### 3.2) Receiver Eye-closure

Figure 7 shows the relationship of the reference clock jitter to the eye-closure seen at the receiver. This is the diagram for a PI type clock recovery. A description of this type of clock recovery can be found in[4].

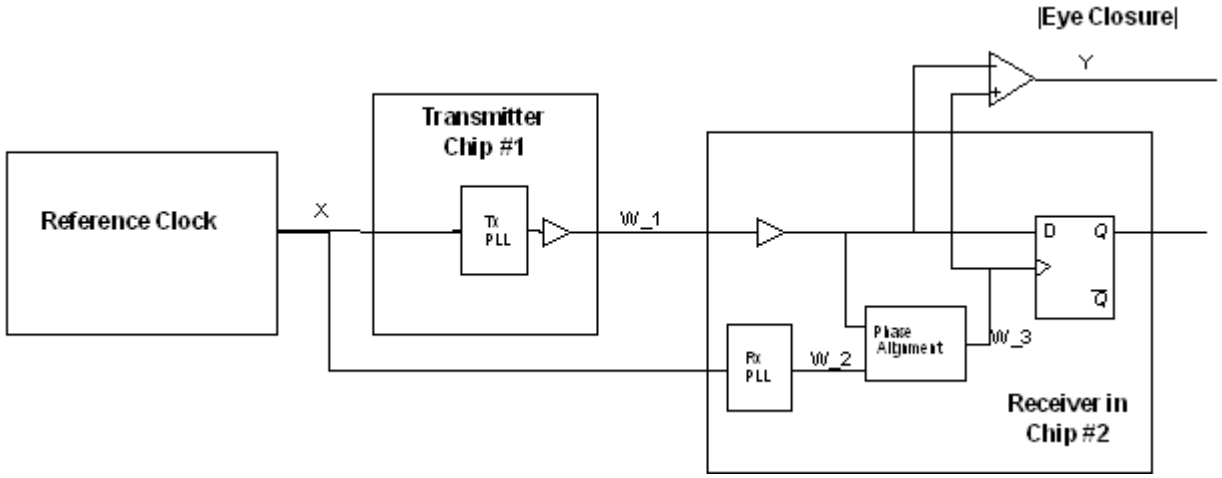


Figure 7: System model for reference clock input X to eye-closure Y for a digital CDRC

For this architecture, the receiver sees phase jitter not as the absolute value of W_1 (input signal to the flip-flop D port), but as the relative difference between W_1 and W_3 (input signal to the flip-flop clock port). The closure is given as Y and consists of all the sources of jitter.

This paper addresses only the jitter that is caused by the mismatch in the PLLs in response to jitter content of X and the bandwidths of the PLLs. There are many other sources of jitter that consume the timing budget at the receiver; these will be explored in some detail in a future paper.

### 3.3) System Transfer Functions

In this section, we will define the model and system transfer function for the PLLs. A review of system transfer functions can be found in references[5][6], from which we adopt the notation conventions used in this paper.

More information on PLL transfer functions and modeling PLLs in the s-domain can be found in references[7][8].

#### 3.3.1) PLL Transfer Function

The input signal to a PLL is

$$V_{in}(t) = A_{in}\sin\left(\omega_{in}t + P_{in}(t)\right) \tag{3.1}$$

and the output signal of the PLL is

$$V_{out}(t) = A_{out}\sin\left(\omega_{out}t + P_{out}(t)\right) \tag{3.2}$$

Here $\omega_{in}$ is the input carrier frequency and $\omega_{out}$ is the multiplied output frequency, both given in radians per second. The terms $P_{in}(t)$ and $P_{out}(t)$, expressed in radians, represent the absolute phase in time of the input and output signals and are sometimes referred to as "excess phase" or, in this discussion, phase jitter. In a properly designed PLL, the input and output frequencies and amplitudes do not change with time. The phase signals $P_{in}(t)$ and $P_{out}(t)$ are a function of time, so the PLL has a phase transfer function. In the complex s domain, the phase transfer function of the PLL H(s) is given by

$$H(s) = \frac{P_{out}(s)}{P_{in}(s)} \tag{3.3}$$

$P_{out}(s)$ and $P_{in}(s)$ are the Laplace transforms of $P_{out}(t)$ and $P_{in}(t)$. The PLL is also a control system that transfers the phase modulation at its input to its output. Knowing the transfer function and the input phase, the output phase can be calculated. Or in general, knowing two of the three functions in equation (3.3), the third one can be estimated through it.

Actual PLLs used in typical CMOS process are often having a third-order transfer functions and the additional pole for the 3rd-order can steep the transfer function magnitude response at high frequencies. However, they can still be approximated as a

second-order transfer function over the bulk of the interested frequency range. This discussion exclusively uses the simpler second-order transfer function as an approximation.

### 3.3.2) Second-Order PLL Transfer Functions

We will use a two-pole, one-zero second-order model for the PLL transfer function. The second order model is based on the active proportional integration control loop with the transfer function given by:

$$H(s) = \frac{2\zeta\omega_n s + {\omega_n}^2}{s^2 + 2\zeta\omega_n s + {\omega_n}^2} \tag{3.4}$$

where $\zeta$ is the damping factor, and $\omega_n$ is the natural frequency. This function is not meant as a requirement for an implementation. It is used as a bounding function for modeling purposes to establish the lower limit for the f_3 dB frequency and the maximum peaking.

The translation between natural frequency $\omega_n$ and the 3 dB frequency is given by:

$$\omega_{3dB} = \omega_n \sqrt{1 + 2\zeta^2 + \sqrt{(1 + 2\zeta^2)^2 + 1}} \tag{3.5}$$

An upper allowed bound of 3 dB of peaking was chosen for analysis in order to limit the resultant worst case gain, resulting in $\zeta$ of 0.54 minimum. This results in the transfer functions shown in Figure 8 for the example where the 3 dB frequency (f_3 dB) is 15 MHz.

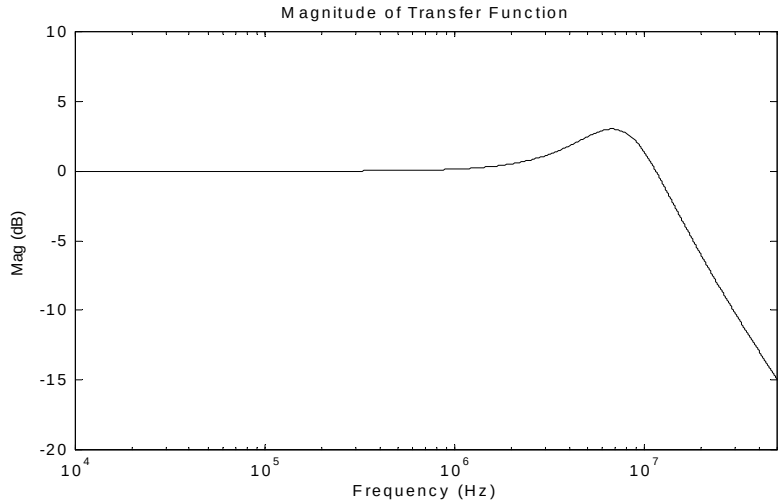


Figure 8: Transfer functions for f_3dB = 15 MHz and $\zeta$ = 0.54

### 3.3.3) Digital CDRC System Transfer Function

Referring to the system model diagram in Figure 7, the input phase jitter signal x(t) is transformed to the s domain as X(s) and is acted on by the transfer functions of the system model as discussed in section 3.3.1. The system model can be simplified and drawn as shown in Figure 9.

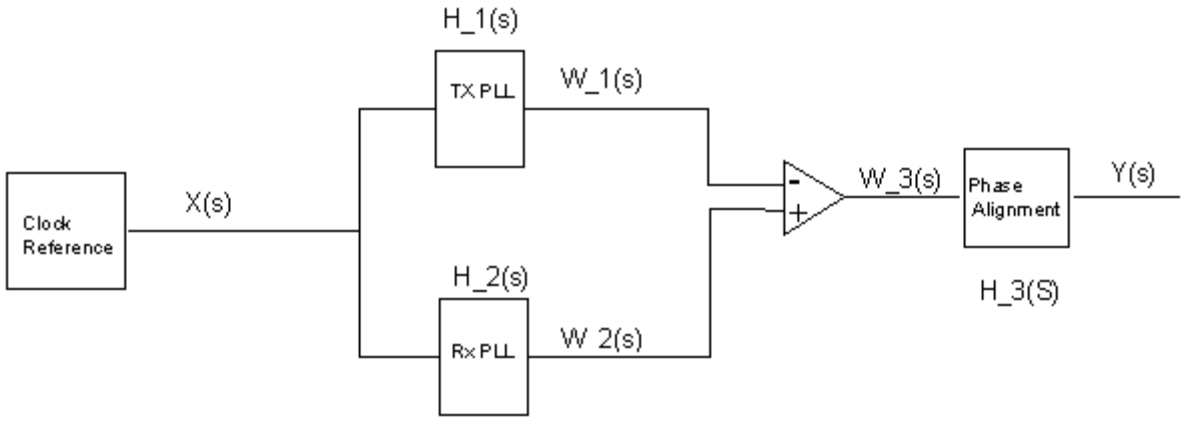


Figure 9: Simplified system model for input jitter to receiver eye-closure

Here X(s) is the input signal representing the input phase jitter, H_1(s) is the transfer function of the Tx PLL, H_2(s) is the transfer function of the Rx PLL, H_3(s) is the high-pass transfer function of the CDRC, and Y(s) is the output signal that represents the eye-closure at the receiver caused only by the jitter on the reference clock propagating through the system.

The total transfer function of this system is given by

$$H_t(s) = [H_{\_1}(s) - H_{\_2}(s)]H_{\_3}(s) \quad \textbf{(3.6)}$$

The output signal can then be calculated for any X(s) as $Y(s) = H_t(s) \bullet X(s)$. Note that there is a phase delay that is not shown and will be discussed in next section.

The transfer function $H_{\_3}(s)$ is the response of the CDRC circuit. $H_{\_3}(s)$ is assumed to have a f3_3dB response of 1 MHz or higher. This is necessary so that the CDRC can track out the phase jitter caused by the combination of SSC (at 33 KHz) and transport delay. The transfer function of $H_{\_3}(s)$ is a single-pole high-pass function that is given by

$$H_{\_3}(s) = \frac{s}{s + \omega_3} \quad \textbf{(3.7)}$$

where $\omega_3$ is simply $\omega_3 = 2\pi\ f3\_3dB$.

It is clear that if $H_{\_1}(s)$ and $H_{\_2}(s)$ are perfectly matched; no eye-closure occurs regardless of the phase jitter content of the reference clock since $H_t(s) = 0$. When there is a mismatch in the transfer function, an eye-closure occurs that is dependent on the phase jitter content of the reference clock and the difference of the transfer functions. In practice, the control of the transfer function is inexact and the variance is large even between two devices of the exact same design, process, and manufacturing lot.

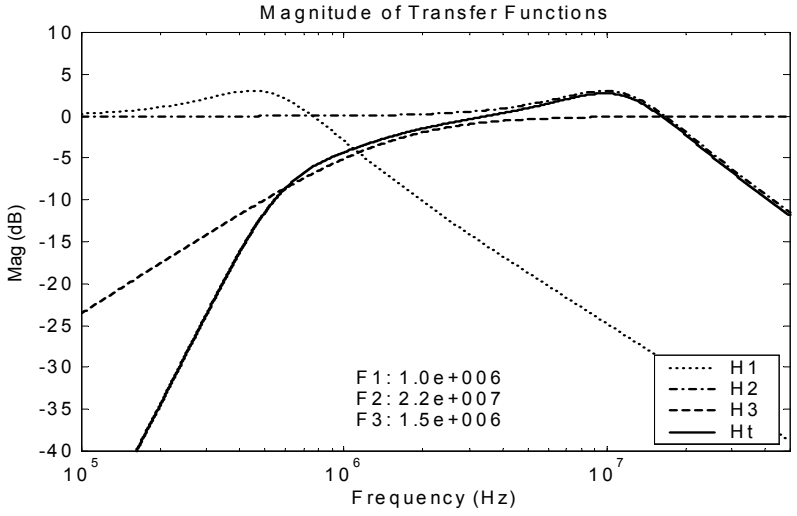

Figure 10: Input jitter to eye-closure for f1_3dB = 1MHz, f2_3dB=22 MHz, and f3_3dB = 1.5MHz and $\zeta_1 = \zeta_2 = 0.54$

Figure 10 gives the transfer function of reference clock phase jitter to receiver eye-closure. All of the phase jitter frequencies present in an input signal X(s) in the frequency range of ~ 400 kHz to ~20 MHz will cause the eye to close at Y(s), with attenuation occurring outside this range. Due to the peaking, there is gain in this range, and the phase jitter gets amplified. Only a portion of the phase jitter outside this range contributes to the eye-closure at Y(s).

This means that low-frequency on the clock reference phase jitter is tracked equally by both the Tx and Rx devices and does not contribute to eye-closure. Jitter at ~ 400 kHz, the f_3 dB lower corner of the band-pass function as shown in Figure 10, transfers ~0.707 of its magnitude to eye-closure. Jitter in the range of approximately 400 kHz to 10 MHz is amplified and contributes directly to eye-closure.

Setting the minimum f1_3dB frequency to 7 MHz for Tx and the maximum f2_3dB set at 22 MHz for Rx, or vice verse, we get the transfer function shown in Figure 11. This is the transfer function that is to be applied to the reference clock phase jitter X(s) to produce Y(s) eye-closure at the Rx in order to model this range of PLLs in the Tx and Rx. The upper limit of 22MHz was chosen as the theoretical limit of stability for a PLL with a 100 MHz input reference[8]. The resulting peak value in y(t) is the peak jitter output of the reference clock.

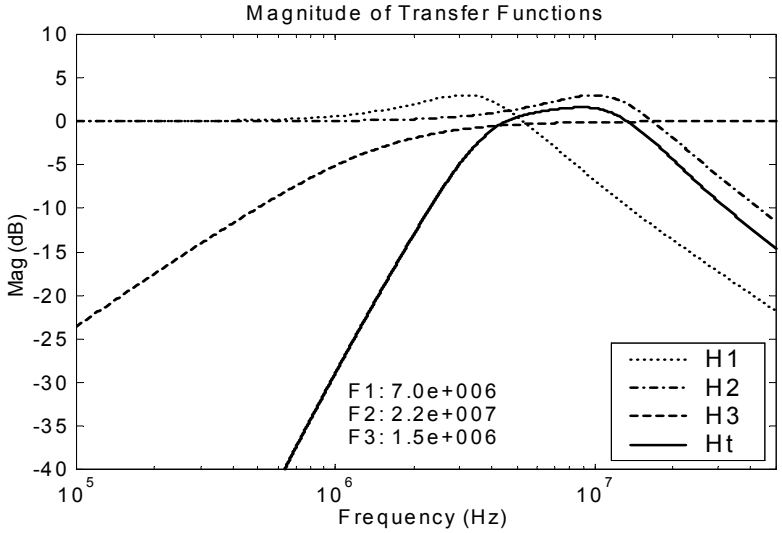


Figure11: Worst case input jitter to eye-closure for f1_3dB = 7MHz, f2_3dB=22 MHz, and f3_3dB = 1.5MHz and $\zeta_1 = \zeta_2 = 0.54$

### 3.3.4) PLL CDRC System Transfer Function

A simplified PLL clock recovery system model is shown in Figure 12 where X(s) is the input phase jitter, H_1(s) is the transfer function of the Tx PLL, H_2(s) is the transfer function for the Rx PLL, and Y(s) is the output.

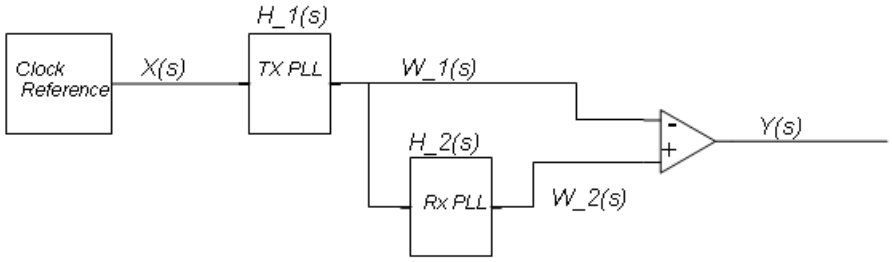


Figure 12: Simplified system transfer function for a PLL based CDRC

The total transfer function is then

$$H_t(s) = H_{\_1}(s)[1 - H_{\_2}(s)] \quad \textbf{(3.8)}$$

In this case, a solution that minimizes $H_t(s)$ is when the 3dB frequency f1_3dB for $H\_1(s)$ is smaller f2_3dB of $H\_2(s)$. Using the PLL transfer function and the frequencies of f1_3dB = 7 MHz and f2_3dB = 22 MHz, the total system transfer function is shown in Figure 13.

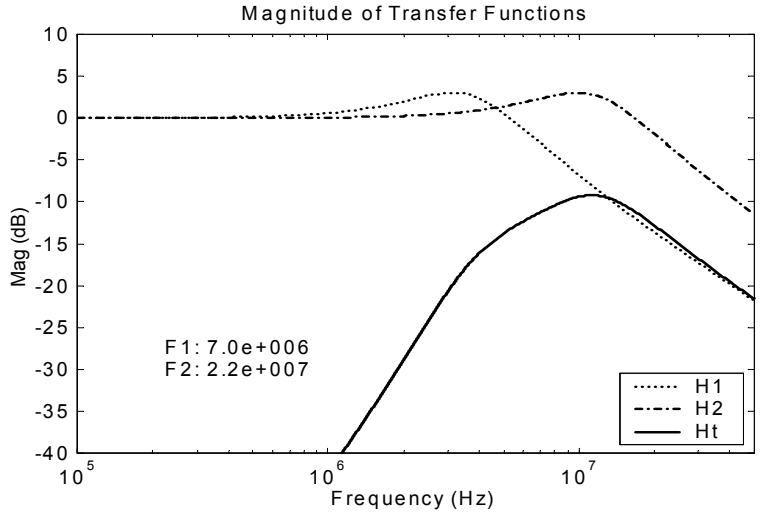


Figure 13: Input jitter to Rx eye-closure for a PLL with f1_3 dB of the Tx PLL at 7 MHz and f2_3 dB of the Rx PLL at 22 MHz

Setting f1_3dB to 22 MHz and f2_3dB to 7 MHz, we get the results shown in Figure 14.

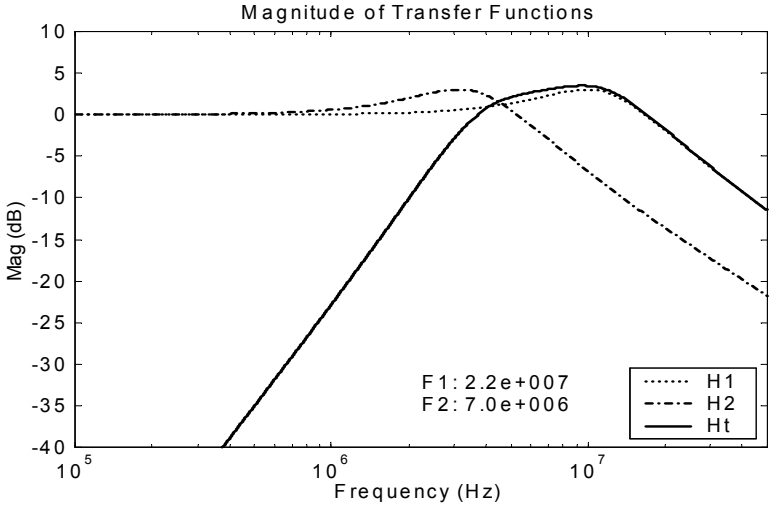


Figure 14: Input jitter to Rx eye-closure for a PLL with f1_3dB of 22 MHz at Tx and f2_3dB of the Rx PLL at 7 MHz

This results in a similar performance as the digital clock recovery model, namely they both show the band-pass characteristic. Clearly the case of having the Rx PLL bandwidth higher than the Tx PLL bandwidth provides better overall jitter rejection. Obviously, to minimize the effect of the reference clock phase jitter it is an advantage for the PLL based CDRC to have a high Rx bandwidth.

### 3.3.5) Transport Delay and System Phase Response

The delay and phase response also contributes to timing error. One component of the phase response is the fixed phase delay due to the routing length differences of the 100 MHz clock and the data channel, as shown in Figure 15. Another component of the phase response is the differences in the transfer functions of the Tx and Rx PLLs. Additional delay may come from the insertion delay of the chips themselves. This is all lumped into the category of phase difference.

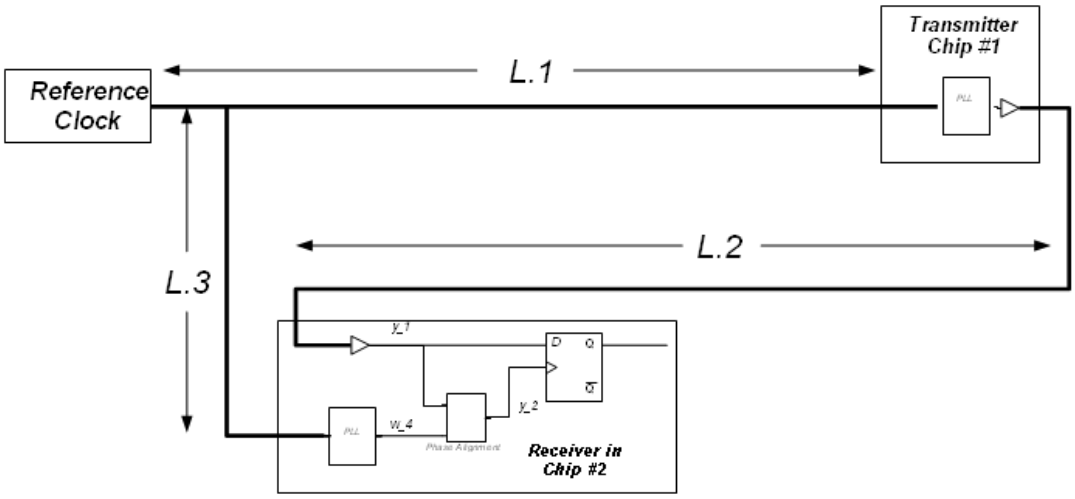


Figure 15: Gain induced by routing phase delay

The phase difference can cause additional eye-closure. The eye-closure can be modeled by multiplying either H_1(s) or H_2(s) by exp(-s•t_delay), where t_delay is the maximum time for the interconnect phase delay and is the relative difference in flight time. This is shown in Figure 15 as [(L1 + L2) – L3] / $v_g$, where $v_g$ is the propagation velocity of the clock signal and is assumed to be a constant. An example of the phase delay effect can be seen in the transfer function as shown in Figure16.

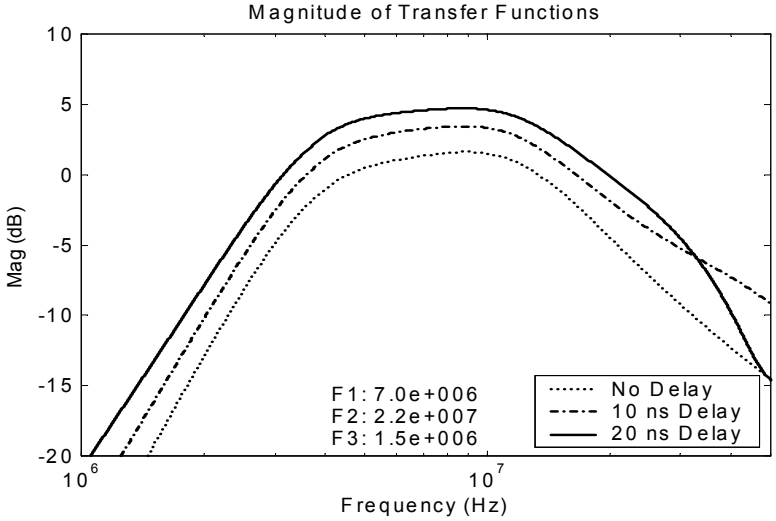


Figure 16: Effect of phase delay on transfer function

We make an assumption that the total delay difference for PCI Express links does not exceed 30 ns, and this is based on the total length of cables that carry the 100 MHz reference clock on a PC board. As the delay between the paths increase beyond 30 ns, the reference clocks become uncorrelated at the higher frequencies and the delay effects become dominant in the transfer functions. In the case of delay beyond 30 ns, the eye-closure can exceed 6 dB at the lower frequencies. The minimum response of $H_{\_3}(s)$ serves to keep the delay effects from dominating the low frequency response. This is shown in Figure 17 where the delayed transfer function, shown in green, rolls off to the left at -40 dB/decade due to the addition of $H_{\_3}(s)$. Without $H_{\_3}(s)$, the delay becomes dominant at the low end and the roll-off is -20 dB/decade.

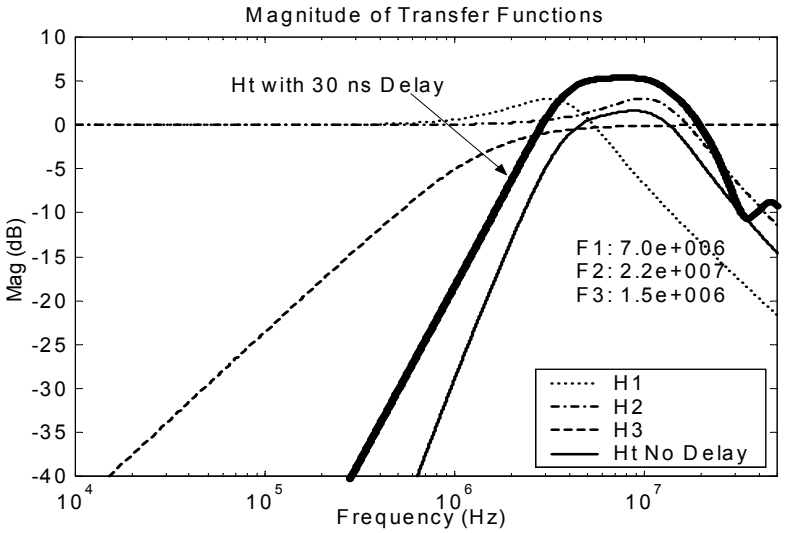


Figure 17 : 30 ns delay effect on eye-closure

# 4.) Applications of Jitter Transfer Function to Platform 100 MHz Reference Clock for PCI Express

The transfer functions developed in section 3 will be used to estimate the eye-closure at the receiver given the phase jitter of the reference clock and the transfer function from the reference clock jitter to receiver eye-closure established in section 3. Due to the page limitation, as well as the fact that most of the PCI Express receivers use digital CDRC, we will only focus on the PI digital CDRC analysis using the theory developed in section 3.3.3, leaving the PLL based CDRC analysis to a future publication using the theory section 3.3.4 and a similar method developed in this section.

One-way to establish the 100 MHz platform reference clock phase jitter upper limit is to identify the maximum amount of jitter after the following transfer function has been applied to the phase jitter and conduct the inverse Laplace transform:

$$y(t) = L^{-1}\{X(s) \times [H\_1(s) - H\_2(s)] \times H\_3(s)\} \quad \textbf{(4.1)}$$

In this example, we use the 3 dB frequency f1_3dB of $H\_1(s)$ as 7 MHz, the 3 dB frequency f2_3dB of $H\_2(s)$ as 22 MHz, and the damping factor $\zeta = 0.54$. H_3(s) is the first order high-pass with a 3 dB frequency of 1.5 MHz. X(s) is the input spectrum of the reference clock and $L^{-1}\{\ldots\}$ is the inverse Laplace transform.

The maximum routing delay as discussed in Section 3.3.5 to account for the worst-case phase delay is accounted for by providing 2x estimation.

The phase modulation of one clock reference chip is shown in Figure 18, where the 33 kHz SS that dominates the phase modulation, can be seen. The SSC component has a magnitude of ~10 ns.

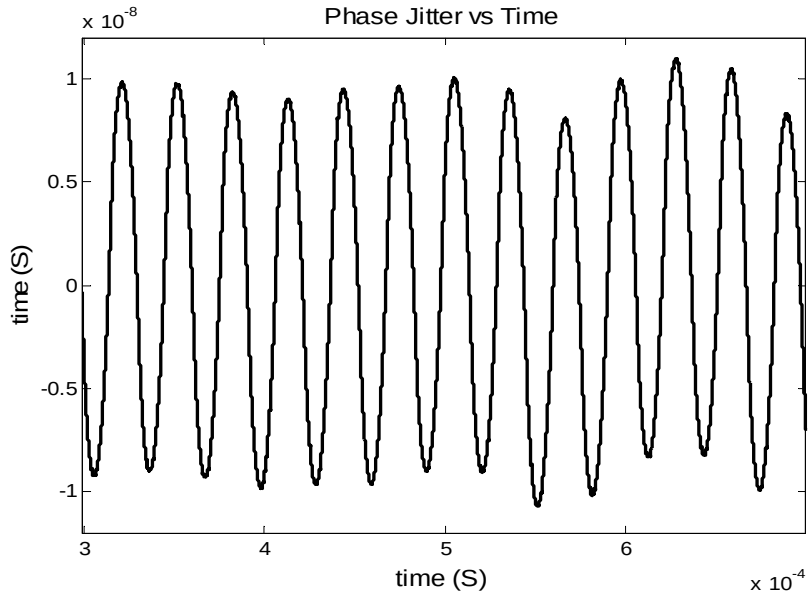


Figure 18: Time-domain phase jitter with SSC as the dominant feature

The spectrum of this reference clock before and after the difference function is applied is shown in Figure 19.

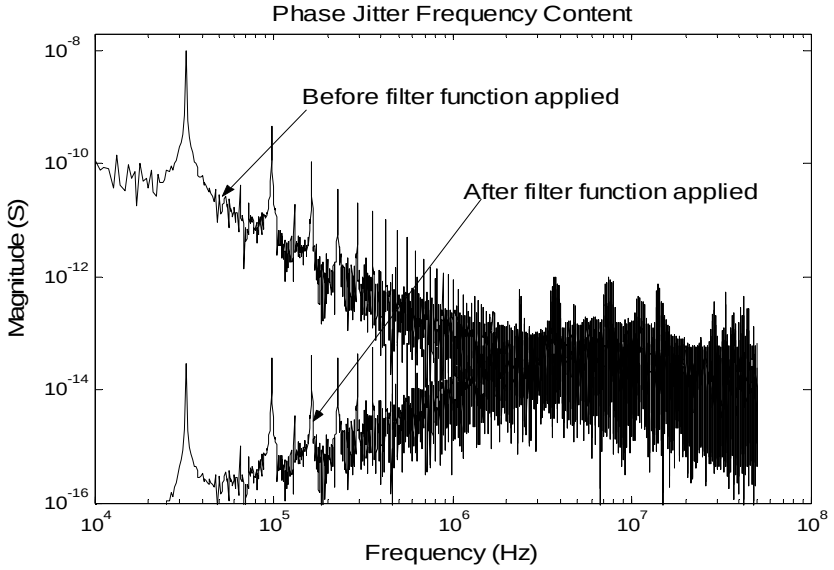


Figure 19: Phase jitter spectrum before and after the system transfer function

The inverse Laplace transform of the spectrum after the difference function of the eye-closure is shown in Figure 20. Here the total eye-closure for this limited sample is on the order of 70 ps.

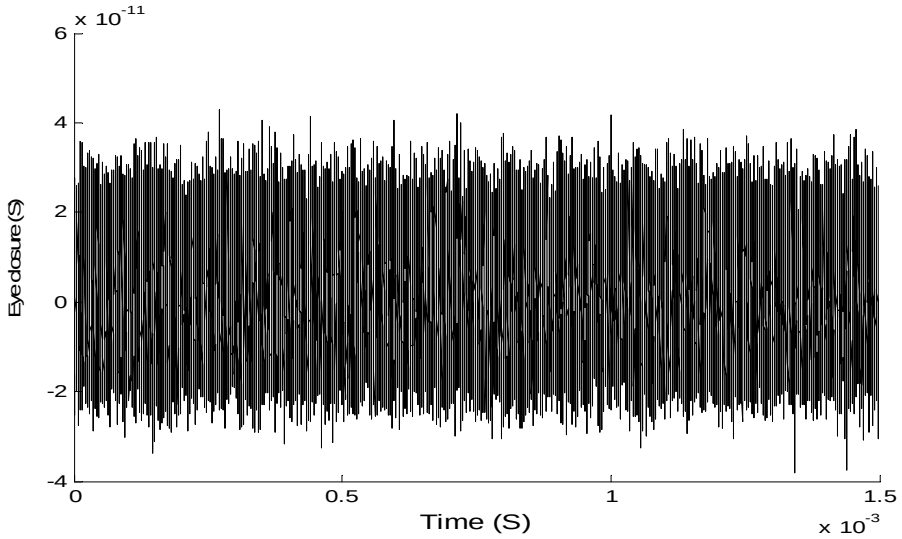

Figure 20: Time-domain of the eye-closure

The phase jitter sample size in Figure 19 and 20 is ~ $1.5x10^5$, giving rise to a BER level of ~$10^{-6}$. The method for establishing an eye-closure down to $10^{-12}$ will be discussed in a future paper.

## 5.) Summary and Conclusions

We have shown that clock jitter can be characterized in a number of ways, phase jitter, period jitter, or cycle-to-cycle jitter. They are different representations of same physical phenomena and therefore are interrelated. Period jitter is equivalent to the first difference of phase jitter, and cycle-to-cycle jitter is equivalent to the first difference of period jitter or the second difference of phase jitter. Given a complete finite record in time of jitter in any one of those three forms, the other two can be derived. However, if only a peak-to-peak value for one form of jitter is known, determination of the peak-to-peak values of the other forms of jitter is *not* possible.

Transfer functions are traditional way of accurately predicting a linear system behavior and they have been developed to model the performance of serial communication system such as PCI Express devices and I/O links when including the effects of reference clock jitter. This paper establishes a method that properly determines the overall performance of the system merited by the eye-closure (or total jitter) at a certain BER, given the reference clock phase jitter and the characteristics of the parts of the system, such as PLL transfer functions.

These methods will serve as a foundation in establishing the requirements for both transmitter and receiver PLL transfer functions and reference clock jitter in way that the eye-closure at the receiver meets certain needs. Without these foundations, it is not possible to establish any rational bound for the reference clock jitter, trade-off between transmitter, medium, and receiver eye-closure budget, and appropriate scalable, and interchangeable jitter measurement methods.

We did not discuss the transmitter and receiver eye-closure estimation and measurement methods for the PCI Express serial link in this paper. Those topics will be discussed in a future publication. However, the ground work that we established in this paper for reference clock are still applicable to transmitter and receiver eye-closure estimation and measurement. In fact, we believe that the method we established here can also serve as a guideline for other computer serial link standards where digital or PLL based CDRC are used, along with a noisy reference clock such as the one with SSC. One example would be Serial ATA.

We realize that we have used a second-order transfer function to model the PLL behavior. Experiments designed to evaluate the accuracy and goodness of the second-order PLL model are in progress by using actual PCI Express link system. If, however, the experiments show too big error, then extension of the current second order PLL to a higher order PLL may be necessary to achieve better accuracy. Consequently, the system jitter transfer function will be modified. Those will be the topics for the future publications. Nevertheless, the basic theory foundation established in the current paper will still apply.

We have used s-domain continuous system transfer function to model the PCI Express I/O link where CDRC operates discretely. It is well known that an s-domain transfer function provides a simple and intuitive approach to model the system behavior and yet still provides a good approximation to a corresponding sampled digital system. For higher order accuracy, a Z-domain transfer function approach is needed and we will address the Z-domain transfer function in a future publication.

We want to emphasis that the method established in this paper of first convert the time-domain phase jitter to s-domain spectrum, then multiply the phase jitter spectrum by the jitter transfer function in s-domain, and then apply the inverse Laplace to their product to get back the time domain eye-closure, is, only one-way to obtain the eye-closure. Other alternative methods are also possible. For example, transfer function can also be represented equivalently by a infinitive impulse response (IIR) filter response function in-time domain, and eye-closure can be estimated *directly* in time-domain given the phase jitter in time-domain for the reference clock. In another example the transfer function can be also equated by a clock recovery circuit function and the phase differences between this recovered clock and the reference clock will give the eye-closure estimation *directly* in time domain. We will address those interesting topics in future publications.

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