A Generic and Higher Order Model For High-Speed Test Interface Analysis and De-embedding

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Wavecrest

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Purposes

- Understand how will a transfer function impact the deterministic jitter (DJ) in a linear system
- Introduce a generic model for quantifying DJ for an I/O path
- Apply the linear system/generic model method to analyze and de-embed a high-speed tester interface/fixture

Outline

- Overview of high-speed I/O testing path
- Review of existing analysis methods
- Introducing a generic, pole/zero based model/analysis method
- Simulation results of the new method
- Application of the generic method to tester high-speed I/O path analysis and de-embedding
- Conclusion

Tester High-Speed I/O Path

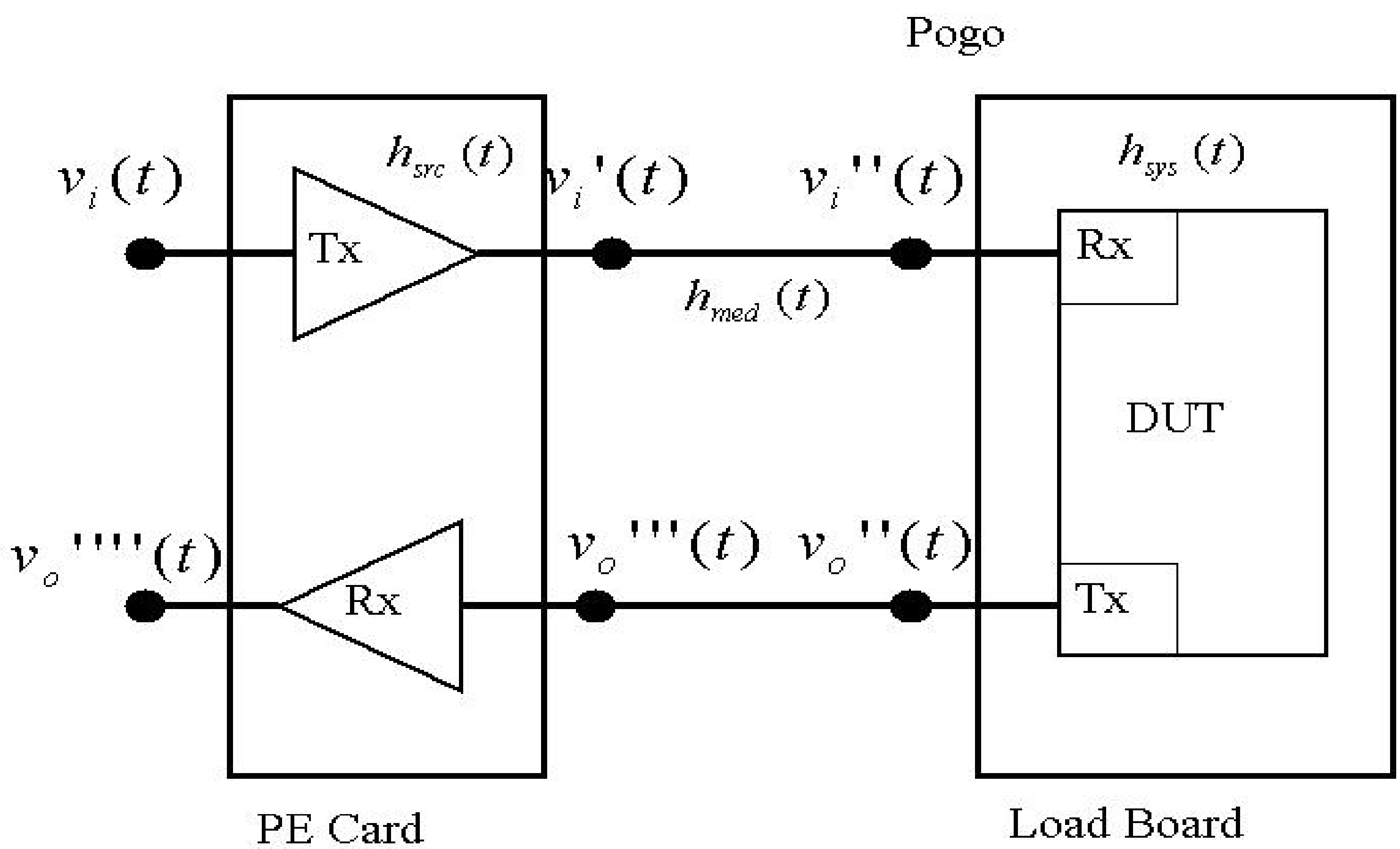
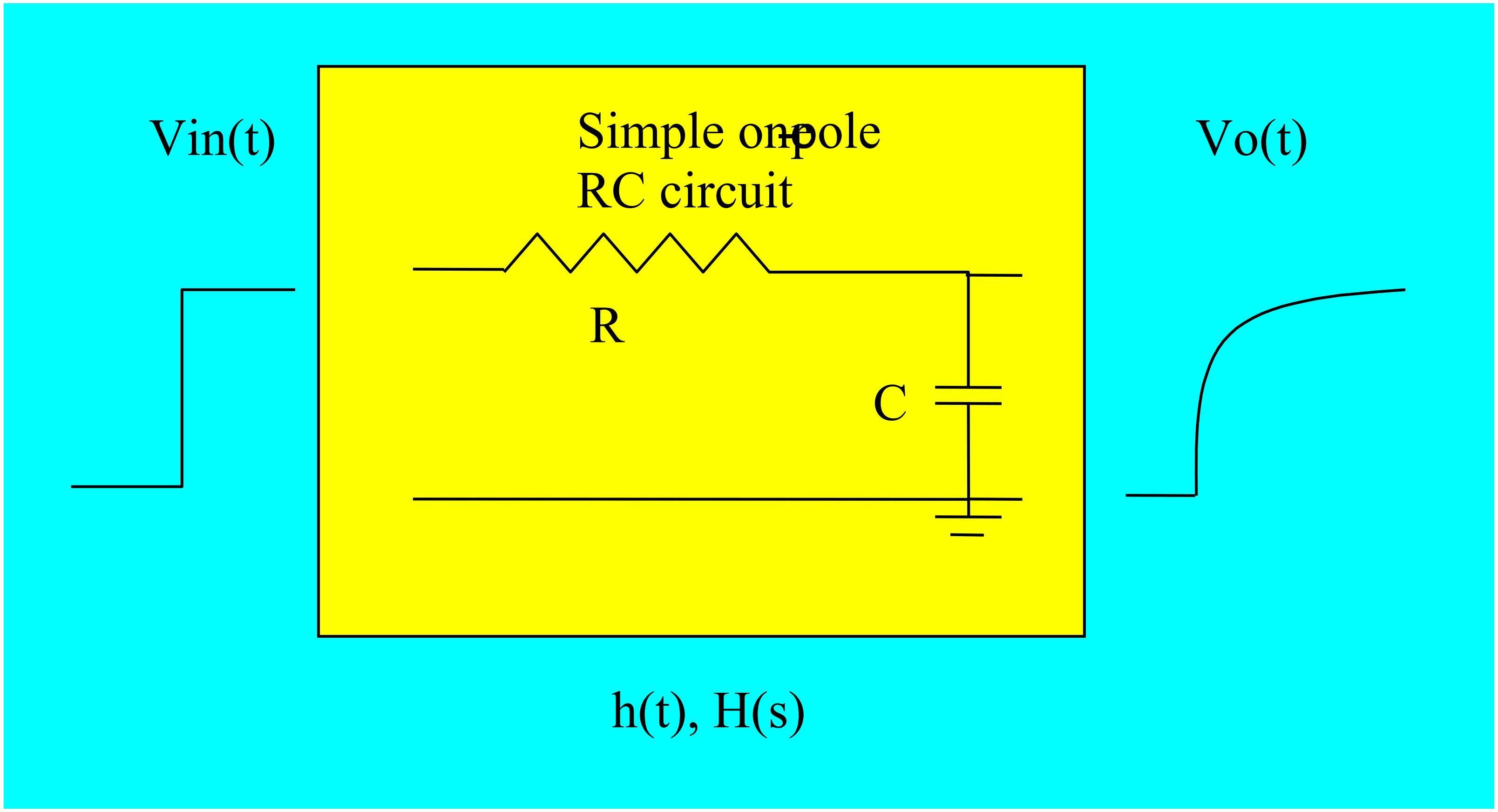


Figure 1. A Typical ATE Setup

Review of A Simple One-Pole System



Limitations of The One-Pole Model

- *Cannot* handle dynamical aspects of the step response (I.e., ringing, damping, overshoot, undershoot etc.)
- *Does not* emulate most of the high-speed I/O paths
- Amplitude ISI effect is shielded

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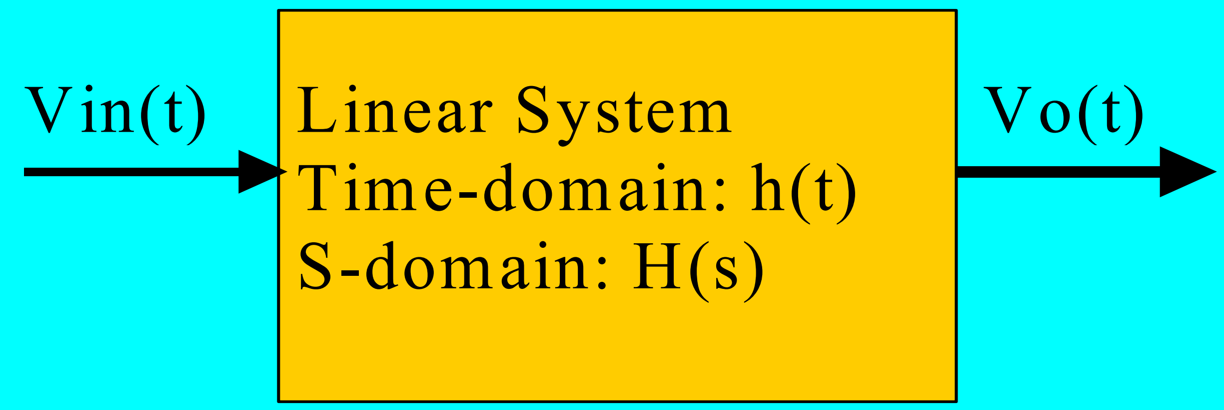
What is Needed?: A Generic, N-pole, M-Zero Model

Goals:

- Eliminate those limitations for the one-pole 1st - order model
- Scalable and generic
- Comprehensive and accurate

Review of Linear System Theory :



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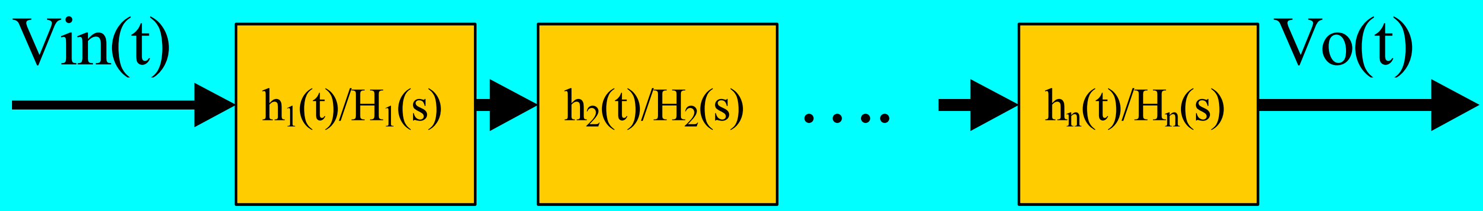
Review of Linear System Theory Cont :

$$H(s) = \int_{-\infty}^{\infty} h(t) e^{-st} dt$$

$$V_0(t) = h(t) * V_i(t) = \int_{-\infty}^{\infty} h(\tau) V_i(t-\tau) d\tau$$

$$V_0(s) = H(s) V_i(s)$$

Independent and Cascade Linear System :



$$h(t) = h_1(t) * h_2(t) * \ldots\ldots * h_n(t)$$

$$H(s) = H_1(s) \bullet H_2(s) \bullet \ldots\ldots \bullet H_n(s)$$

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A Generic N-Pole, M-Zero Model

$$H(s) = K\frac{s^{M} + a_{M-1}s^{M-1} + \cdots + a_0}{s^{N} + b_{N-1}s^{N-1} + \cdots + b_0}$$

$$= K\frac{\prod_{m=1}^{M}(s + z_m)}{\prod_{n=1}^{N}(s - p_n)}$$

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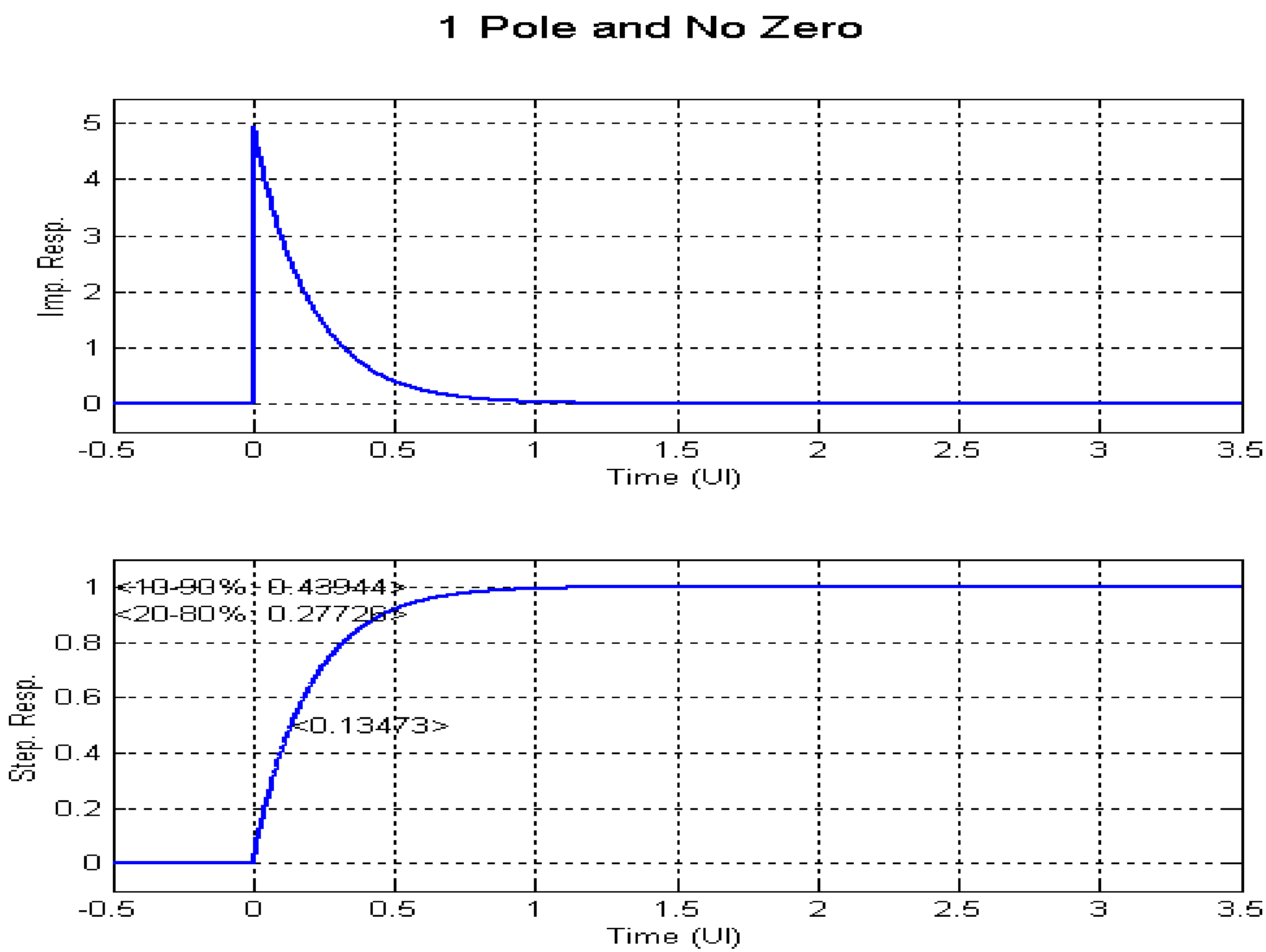
Requirements for a Generic Model

- It must be stable, i.e., all the poles are located on the left half of the *S*-plane, and the number of poles is >= the number of zeros

- It must be causal, i.e., the region of convergence (*ROC*) is right to the rightmost pole

Case Study I:
1-Pole, 0-Zero (Time-domain)



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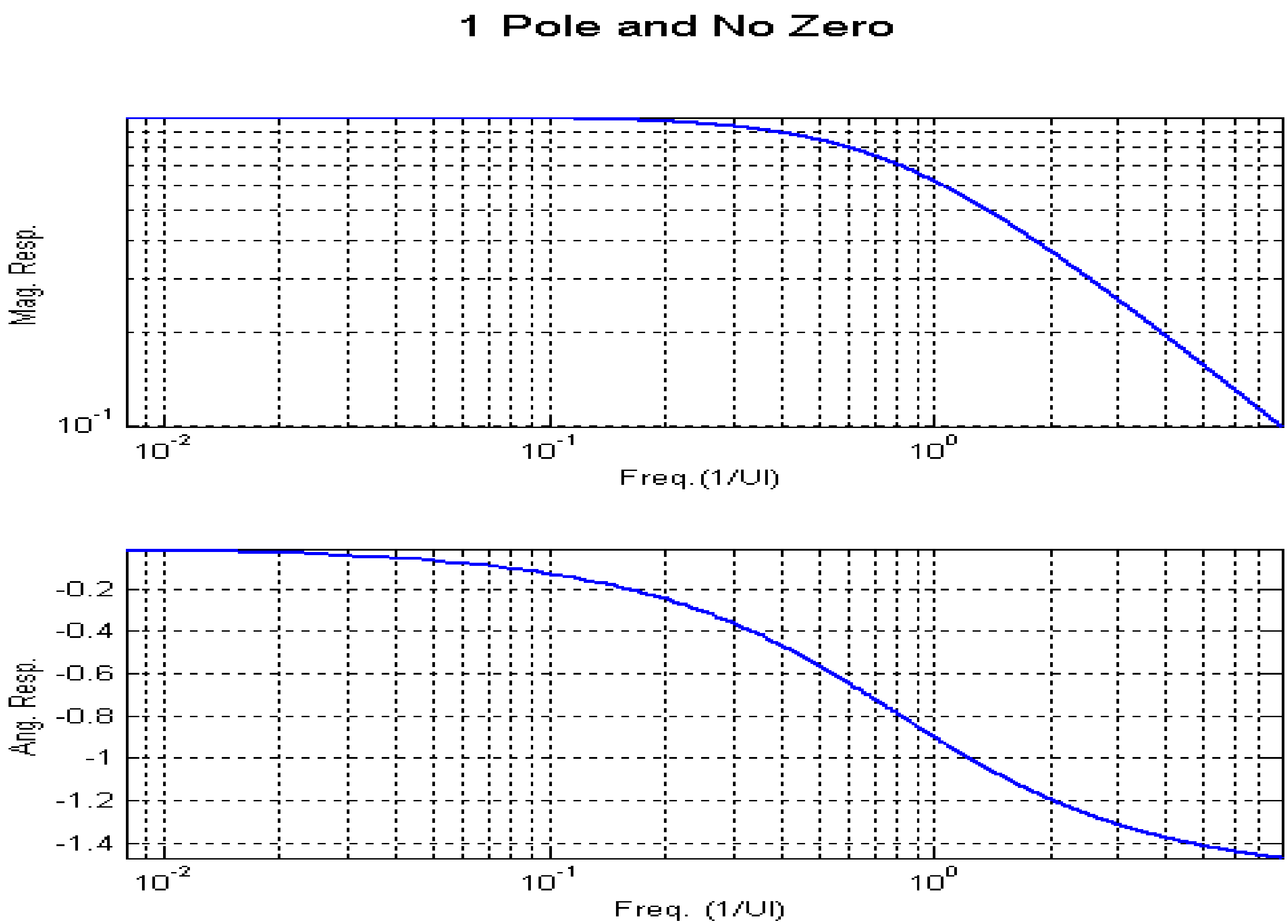
Case Study I: 1-Pole, 0-Zero Cont.. (Frequency-domain)



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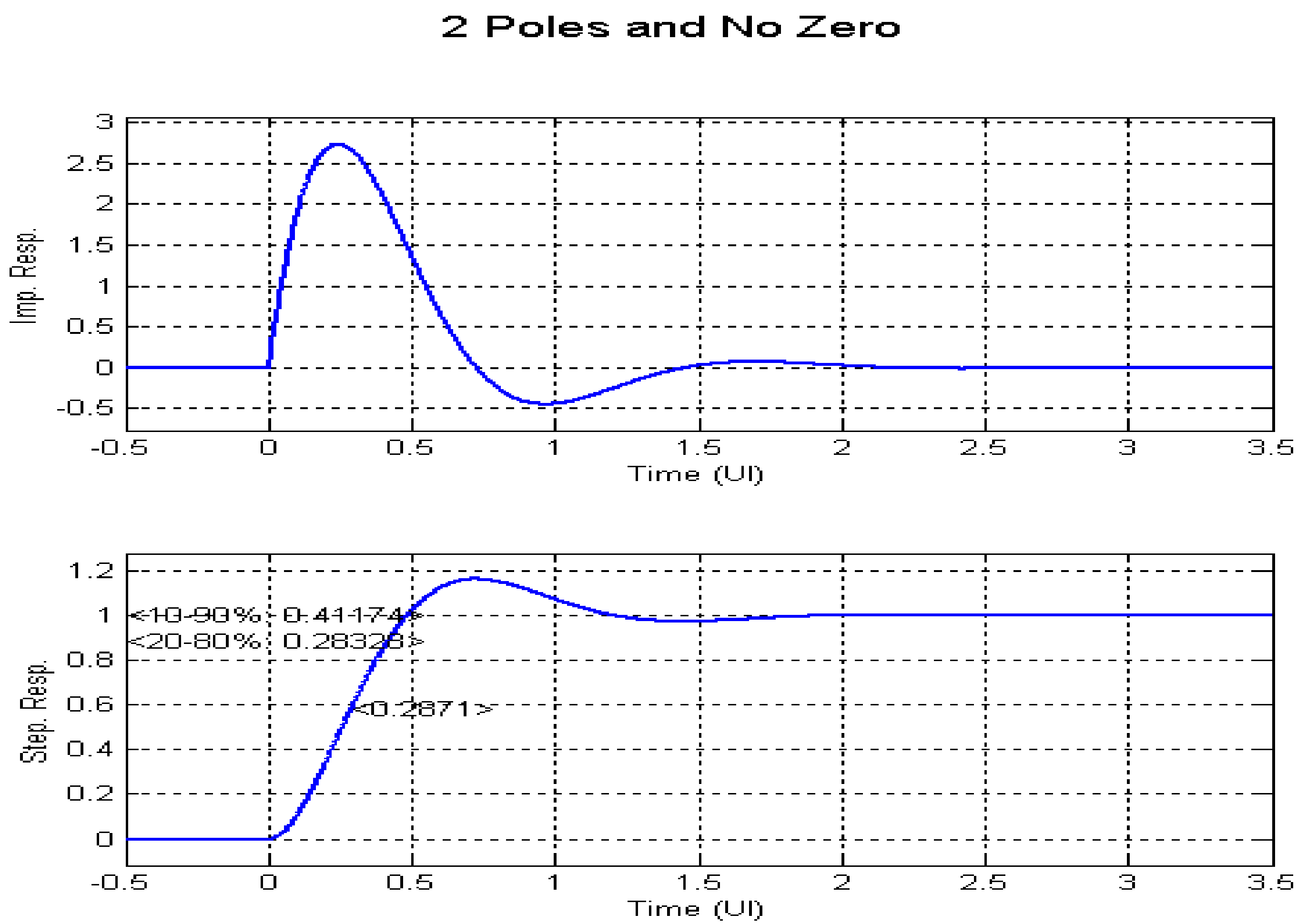
Case Study II: 2-Pole, 0-Zero

(a) Under Damped



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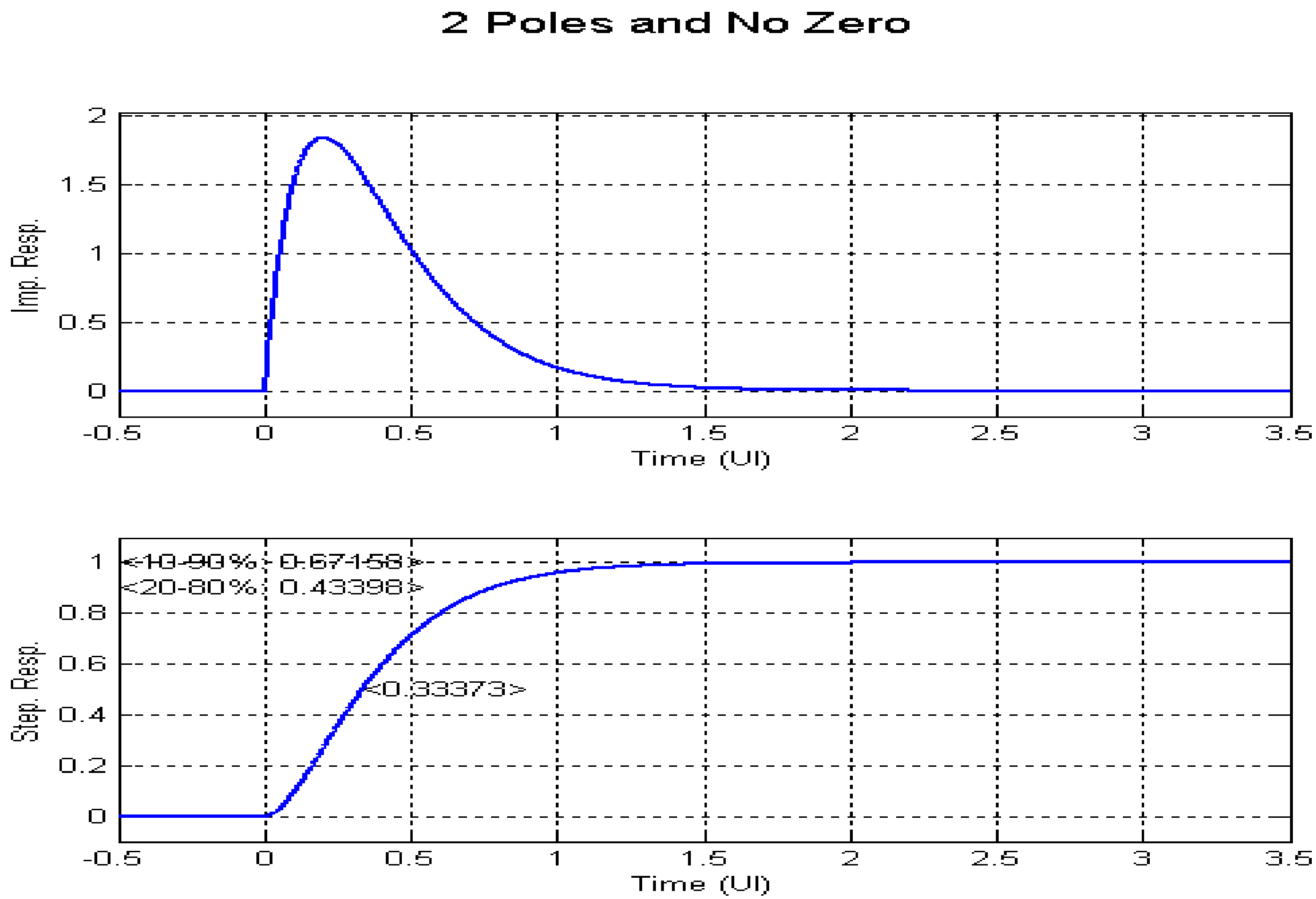
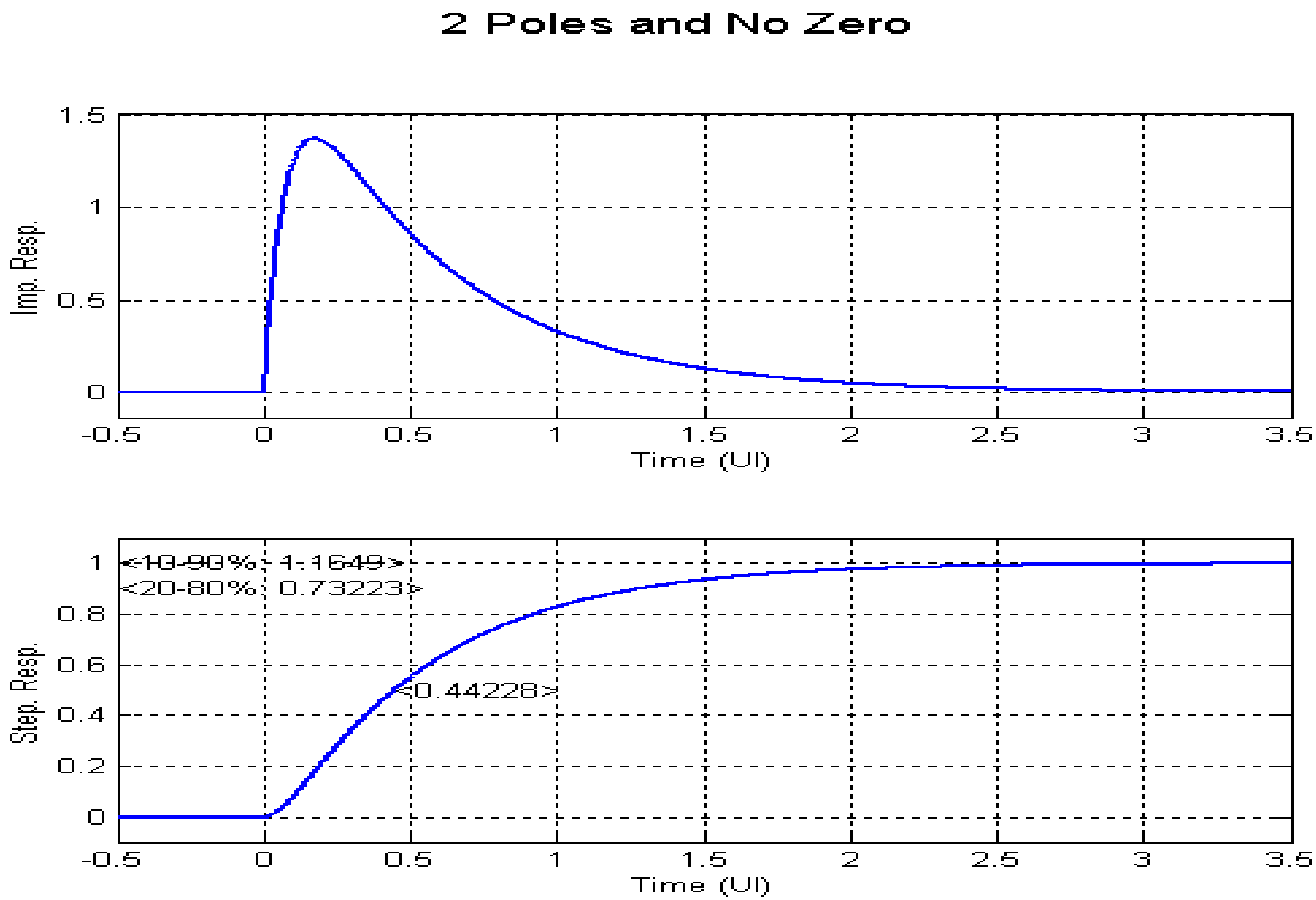
Case Study II: 2-Pole, 0-Zero Cont..

(b) Critically Damped



Case Study II: 2-Pole, 0-Zero Cont..

(c) Over Damped



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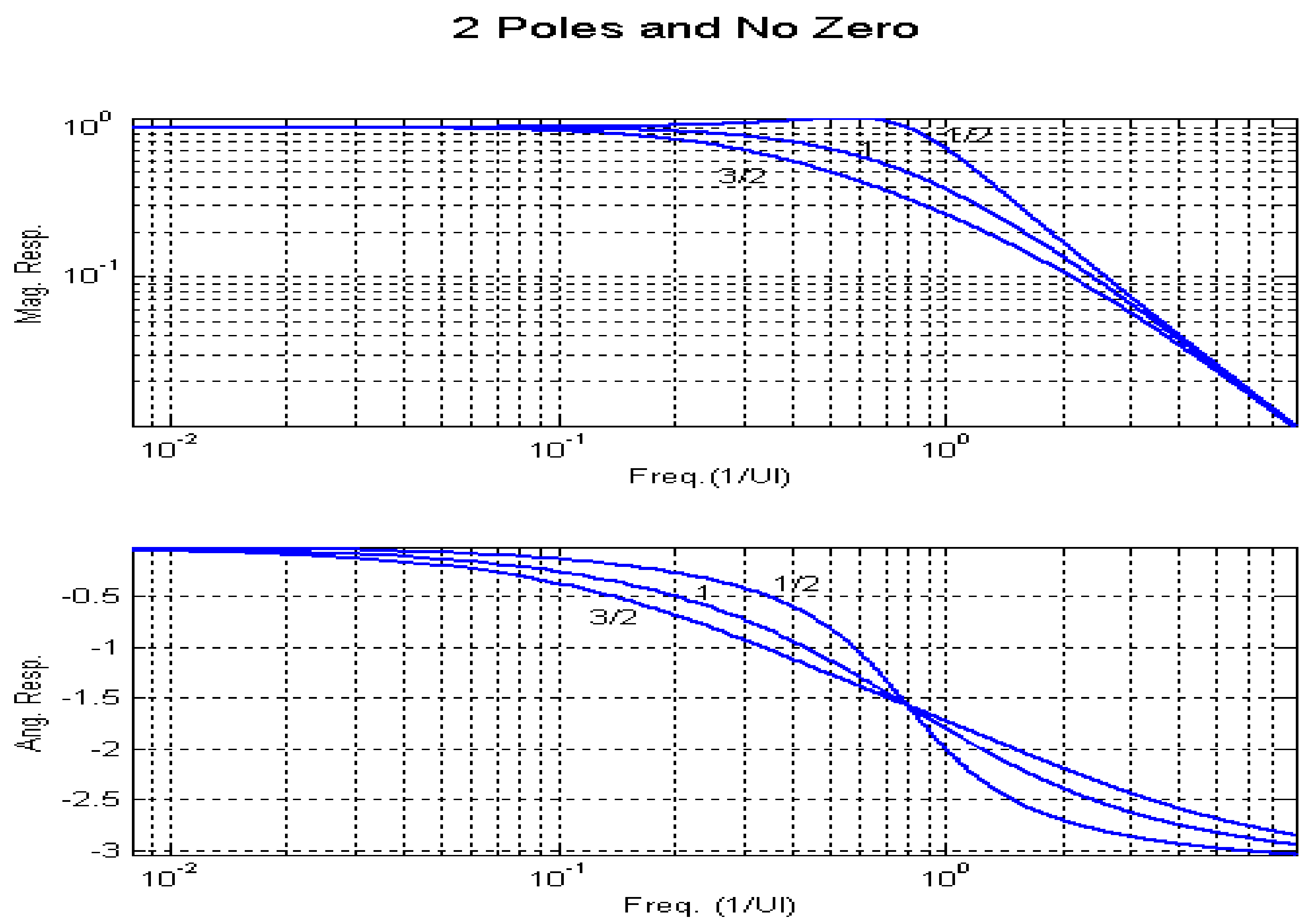
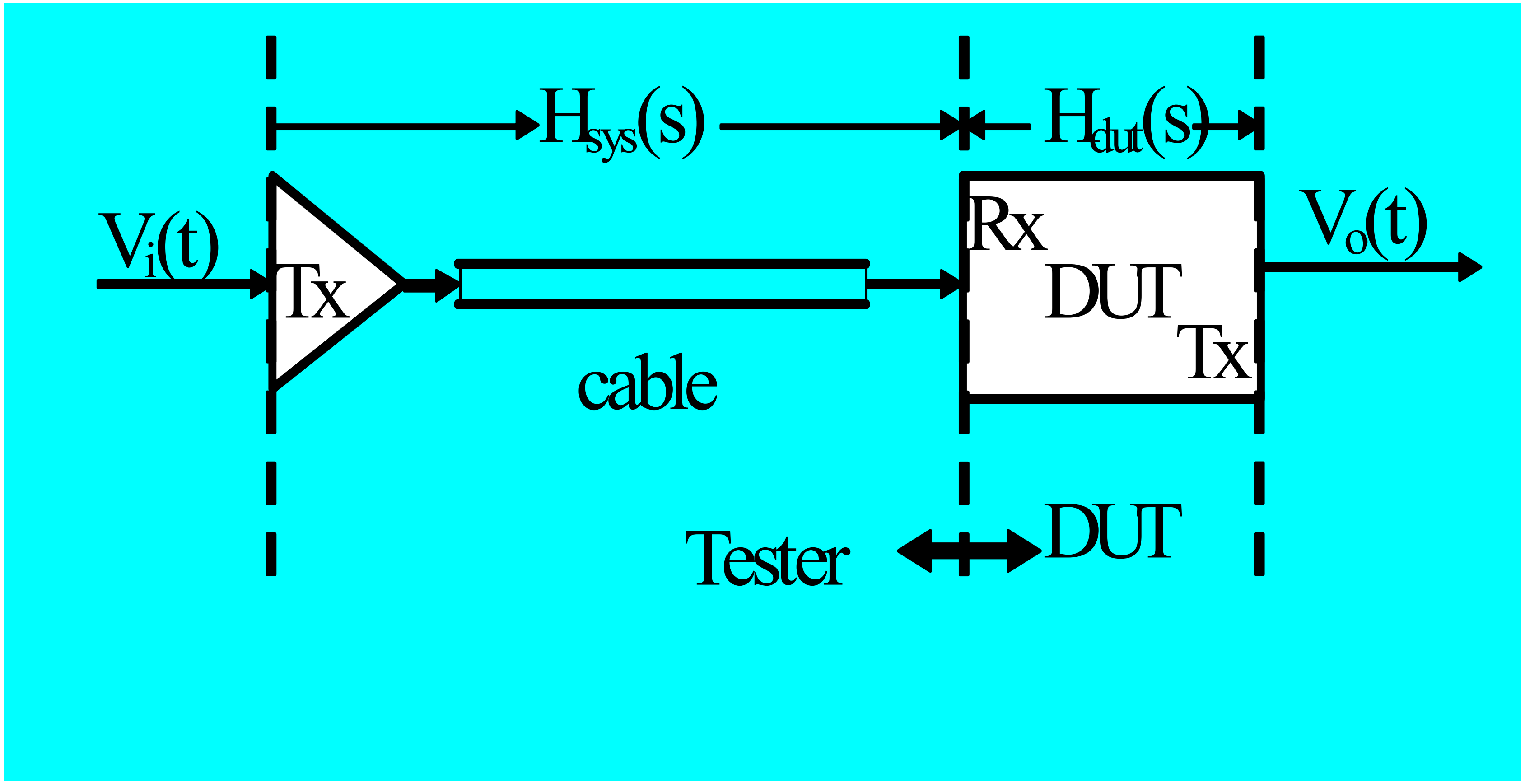
Case Study II: 2-Pole, 0-Zero Cont..



Application to Tester DUT Path



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Modeling Setup

$$H_t(s) = H_{sys}(s) \bullet H_{dut}(s)$$

$$h_t(t) = L^{-1}(H_t(s)) = \frac{1}{2\pi j}\int_{\sigma - j\omega}^{\sigma + j\omega} H_t(s)e^{st}\,ds$$

$$V_0(t) = h_t(t) * V_i(t)$$

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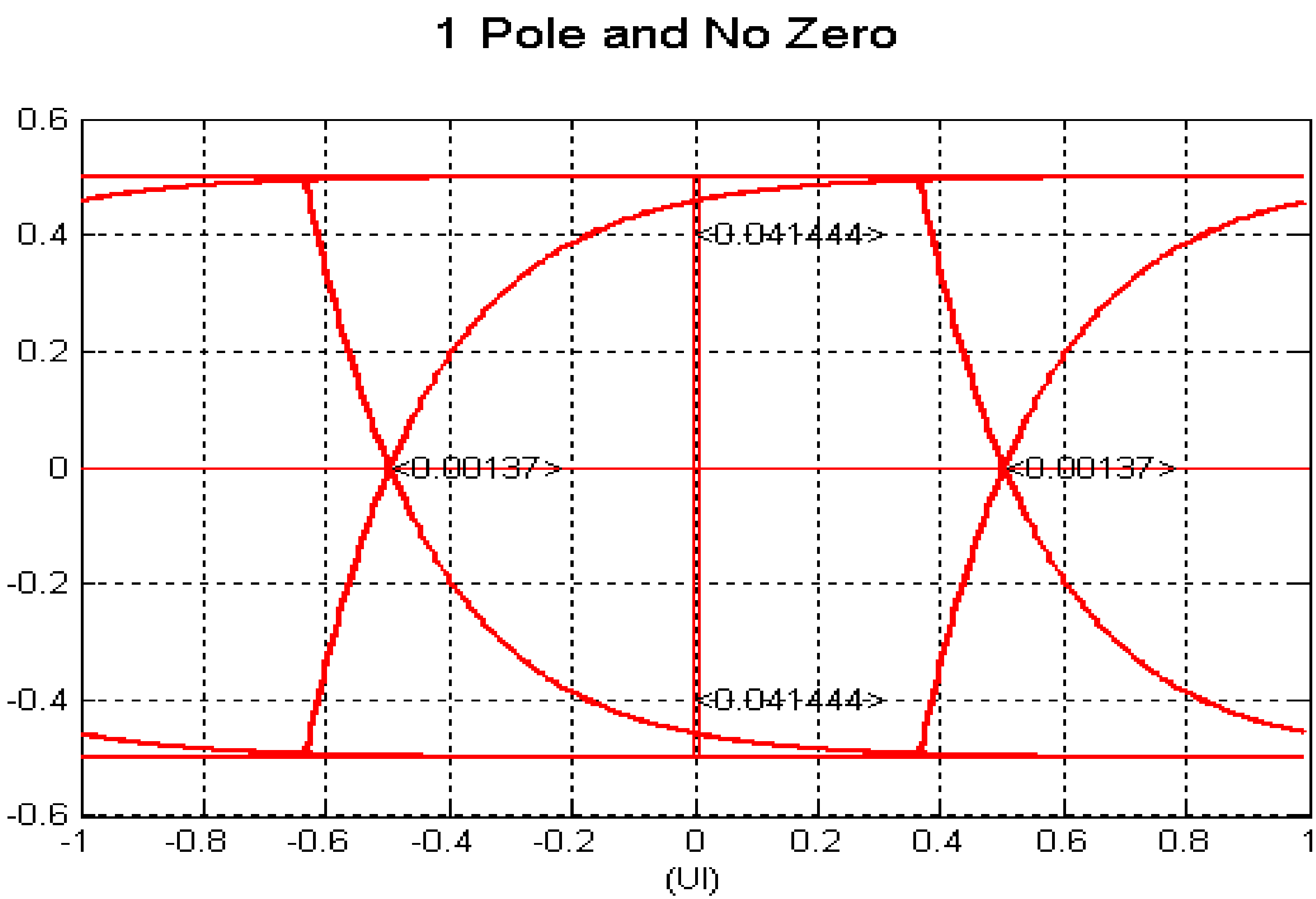
Condition Settings

- $H_{dut}(s)$: assumed to be a 1st-order (1-pole), this is the baseline
- $H_{sys}(s)$: can be a 1st-order or a 2nd-order (1-pole, or 2-pole)
- $H_t(s)$: will be a 2nd-order or a 3rd-order (2-pole or 3-pole)
- $V_i(t)$: Datacom (K28.5, PRBS, CJTPAT) testing patterns

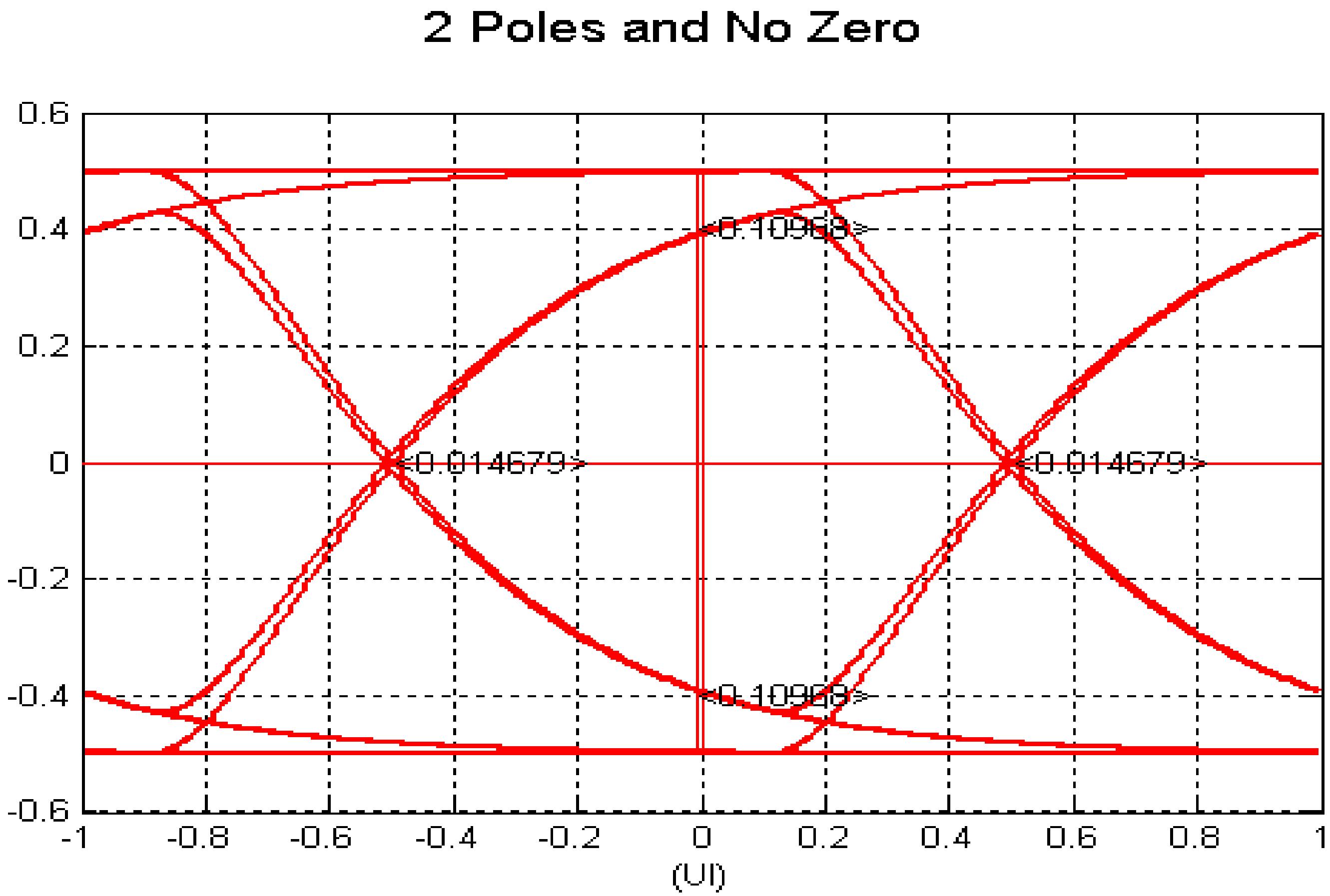
DUT Baseline Eye-Diagram

- $V_i(t)$: K28.5, $H_{dut}(s)$: 1^{st}-order (~ 1 UI Settling)



Effects of "Bandwidth"

- $V_i(t)$: K28.5, $H_{dut}(s)$: 1st –order (~1 UI settling), $H_{sys}(s)$:1st –order (~2 UI settling)



$V_o(t)$ eye-diagram

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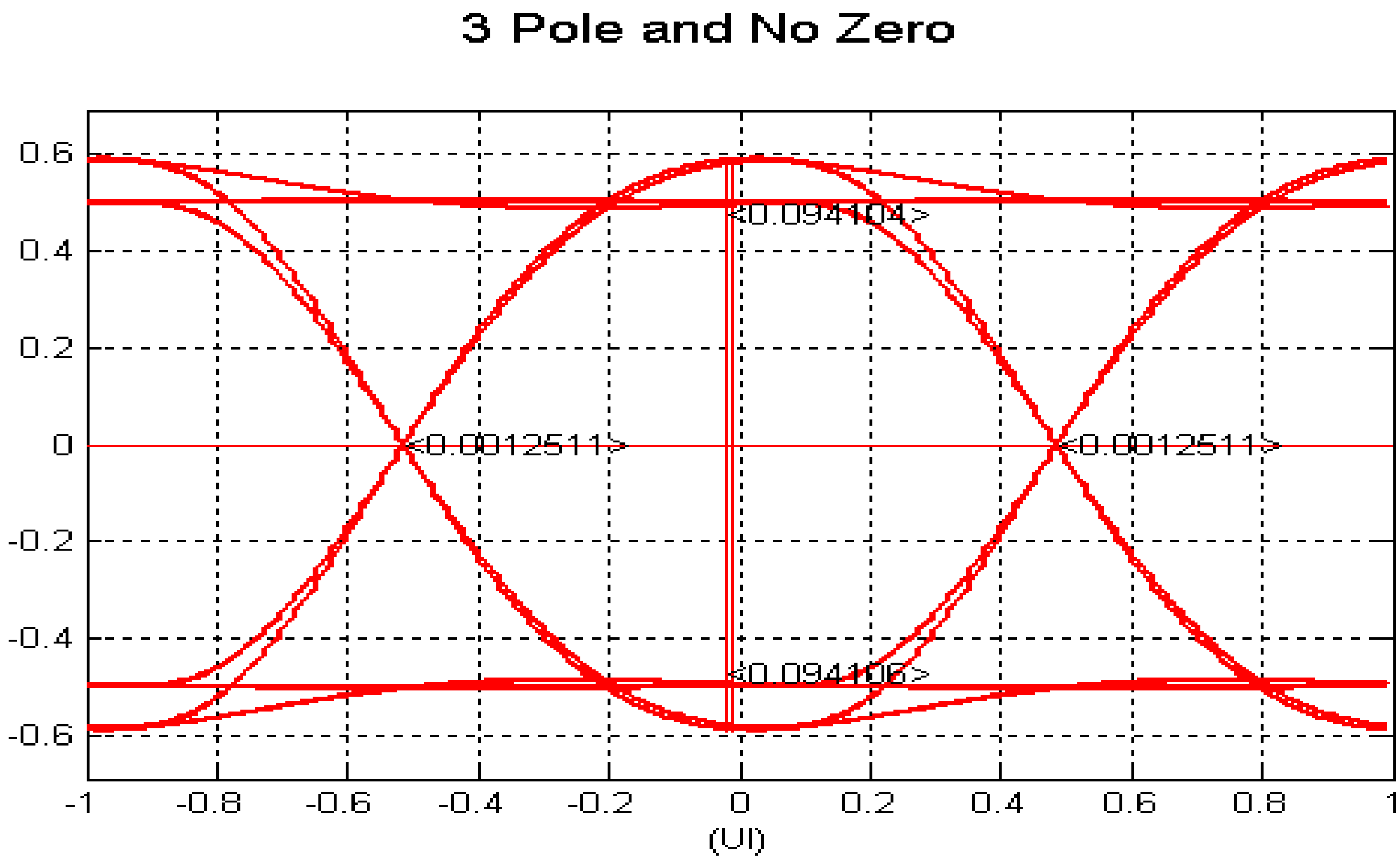
Effects of Ringing

- $V_i(t)$: K28.5, $H_{dut}(s)$: 1st –order (~1 UI settling), $H_{sys}(s)$: 2nd –order (~2 UI settling)



$V_o(t)$ eye-diagram

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Summary Table for "Bandwidth" and Ringing Effects

	DUT	Effect of Tester "Bandwidth"		Effect of Tester Ringing	
		Total	Tester Induced	Total	Tester Induced
Timing ISI (UI)	0.0014	0.015	0.014	0.0013	-0.001
Voltage ISI (UA)	0.041	0.11	0.11	0.095	0.07

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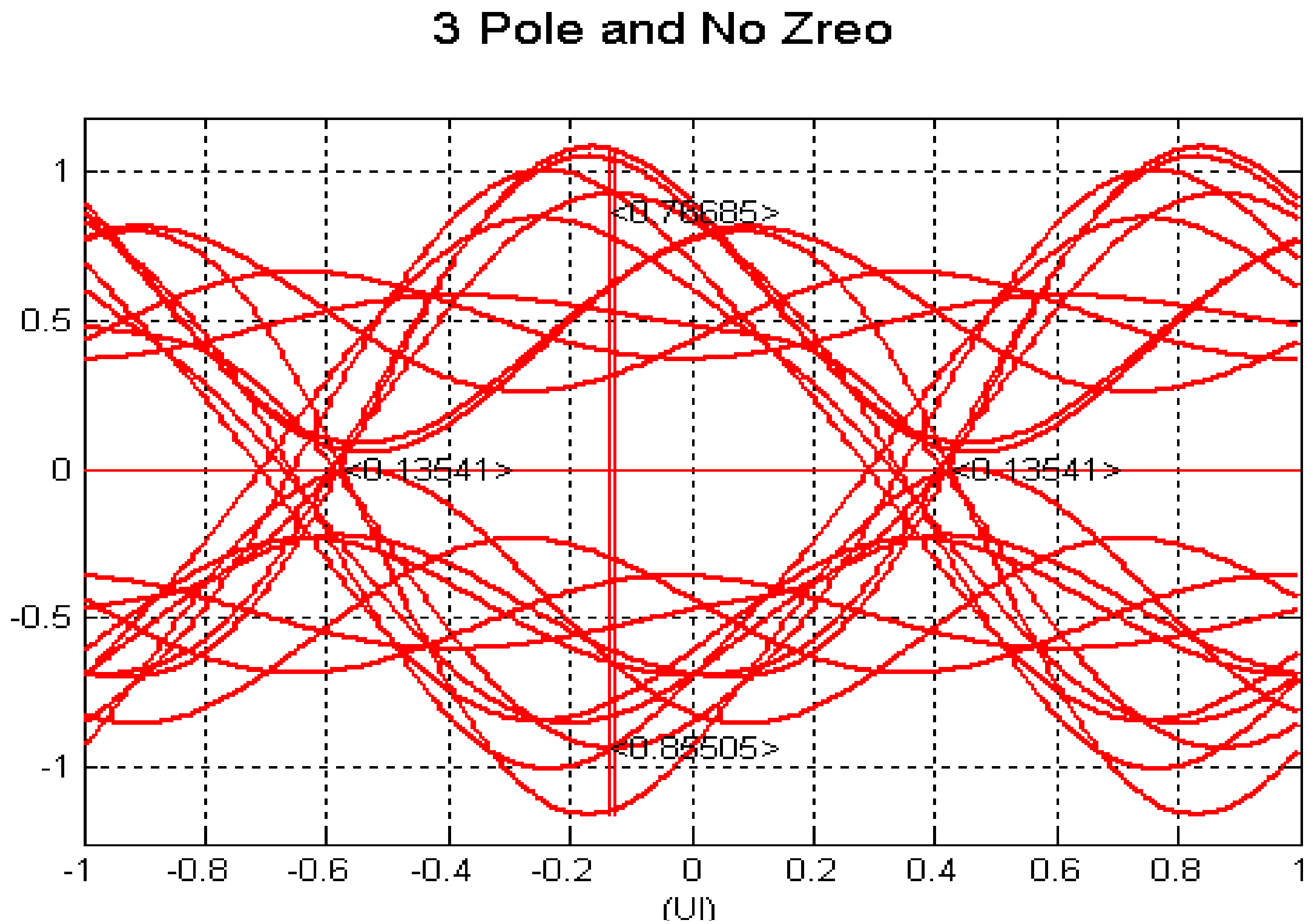
Effects of Data Pattern: K28.5

- $V_i(t)$: K28.5, $H_{dut}(s)$: 1^{st} – order (~ 1 UI settling), $H_{sys}(s)$: 2^{nd} –order (~ 8 UI settling)

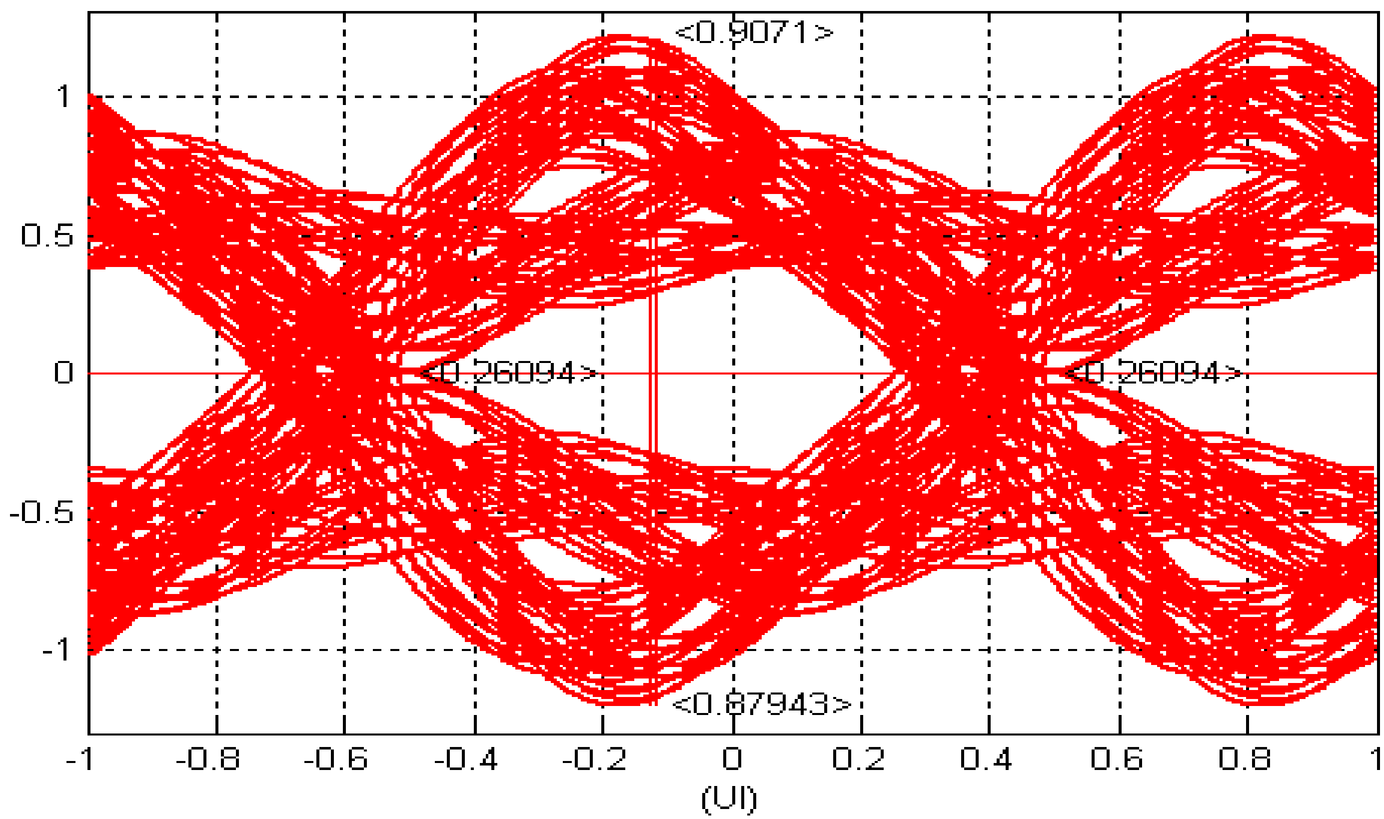


$V_o(t)$ eye-diagram

Effects of Data Pattern: PRBS2^{10}-1

- $V_i(t)$: PRBS2^{10}-1, $H_{dut}(s)$: 1st – order (~ 1 UI settling), $H_{sys}(s)$: 2nd –order (~8 UI settling)

3 Pole and No Zreo



$V_o(t)$ eye-diagram

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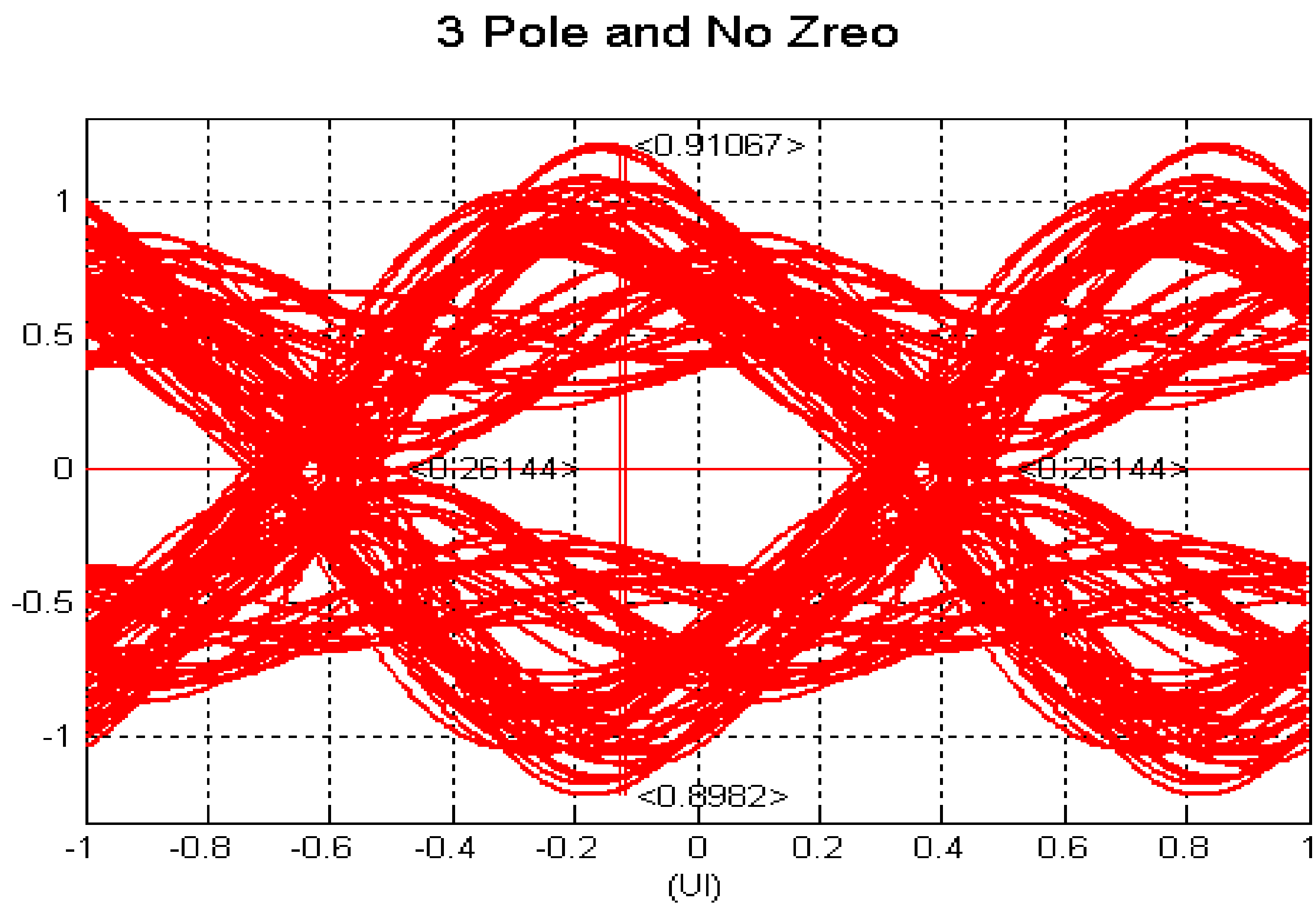
Effects of Data Pattern: CJTPAT

- Vi(t): PRBS2^{10}-1, $H_{dut}(s)$:1^{st} – order (~1 UI settling), $H_{sys}(s)$: 2^{nd} –order (~8 UI settling)



$V_o(t)$ eye-diagram

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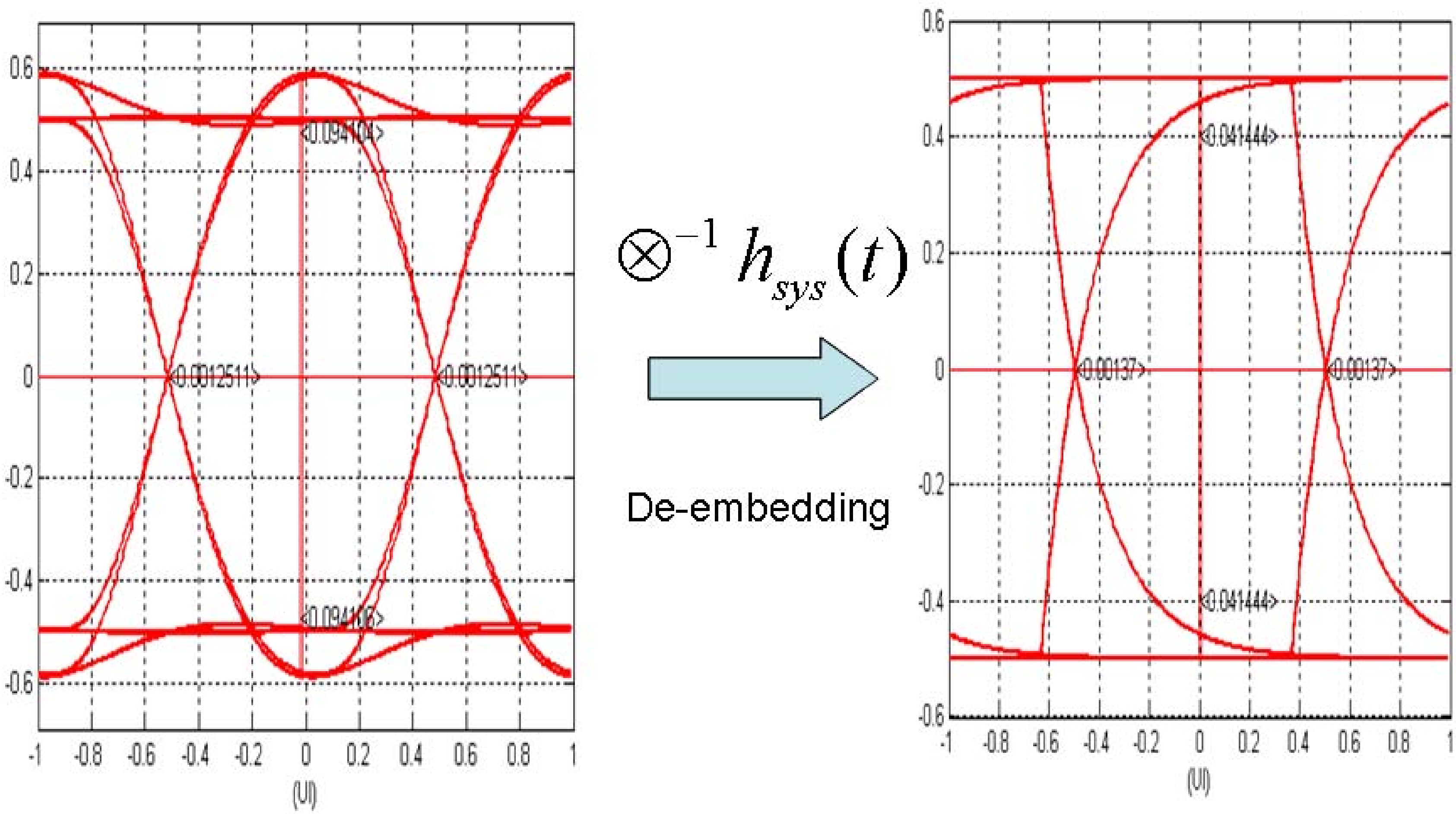
Summary Table for Different Pattern Effects

	K28.5	PRBS $2^{10}-1$	CJTPAT
Timing ISI (UI)	0.14	0.26	0.26
Voltage ISI (UA)	0.86	0.91	0.91

Tester Path Impacts De-embedding



Summary and Conclusion

- A generic Nth-order (or N-pole, M-zero) model is established
- The generic model eliminates all the limitations of the simple, commonly used 1st – order (1-pole) model (see references in the paper)
- Scalability and completeness aspects of the generic model are demonstrated
- Application of the generic model in Datacom Tester I/O path is illustrated
- A tester path effect de-embedding is presented