DesignCon 2007

TecForum

Recent Developments in Jitter and Signal Integrity Measurement and Analysis at Multiple Gbps or GHz

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Abstract

As the speed of mainstream computer interfaces exceed 1 Gbps, conventional synchronized global clock based architecture is replaced by asynchronous serial data communication where the clock is recovered at the receiver by a clock recovery unit. In this tech forum, we will talk about the latest developments in computer communication standards like PCI Express, FB DIMM, Serial ATA, as well as conventional network standards such as Fibre Channel, Giga Bit Ethernet, and SONET. We will review the basic architectures of these interfaces and how to determine the jitter/noise transfer functions for each link. We will then demonstrate how to measure and analyze jitter, noise, and BER (JNB) for various multiple Gb/s links devices for compliance purposes, as well as diagnostic and debug purposes. New emerging test requirements such a pulse width shrinkage (PWS), and de-emphasis jitter removal are discussed and the corresponding test methods/solutions are presented.

Presenter's Biography

Dr. Mike Li is the Chief Technology Officer (CTO) with Wavecrest. ***Dr. Li pioneered jitter separation method (Tailfit) and DJ, RJ, and TJ concept and theory formation. Currently he is Co-Chairman for PCI Express jitter standard committee***. Dr. Li has more than 15 years of high-speed related measurement instrumentation, testing, and analysis experience in applications including IC, microprocessor, clock and serial data communications for electrical and optical, and wireless communication. He has a BS in physics from University of Science and Technology of China, a MSE in electrical engineering and a Ph.D. in physics from University of Alabama in Huntsville. He did his Post Dr. at University of California, Berkeley and worked there as a research scientist on high-energy astrophysics before he joined industry. ***Dr Li has published more than 70 papers in refereed technical journals; holds 4 patents and has 8 patents pending, authored/edited one book on multiple Gb/s design and test.***

Overview

I: **Signal Integrity/Jitter Basics**
- Why separate jitter components?
- Jitter math review
- Probability Density Functions (PDFs), Convolution, and Cumulative Density Functions (CDFs)

II: **Jitter and Signaling Analysis and Test in Serial Datacom**
- Different types of jitter measurements
- How Phase Jitter, Period Jitter and Cycle-to-Cycle Jitter relate
- Jitter transfer functions
- How recovered clocks affect jitter “seen” by the receiver

III. **Link Architecture and Jitter**
- Link architecture review
- Link transmitter, receiver, reference clock, medium jitter test

IV. **Generic Jitter and Signaling Test Requirements and Methods**
- Requirements
- Methods

V. **Jitter and Signaling Test in Gbps Link Standards**
- Fibre Channel (4.25, 8.5 Gbps)/SAS (3, 6 Gbps)
- PCIe (2.5, 5 Gbps)
- FB DIMM (3.2, 4.0, 4.8 Gbps)
- SATA (1.5, 3, 6 Gbps)
- Test solution case studies and illustrations

VI. **Signal Integrity and Jitter for Test Instruments**
- Bandwidth and step response
- Test coverage and performance

VII. **Summary**

I: Signal Integrity and Jitter Basics

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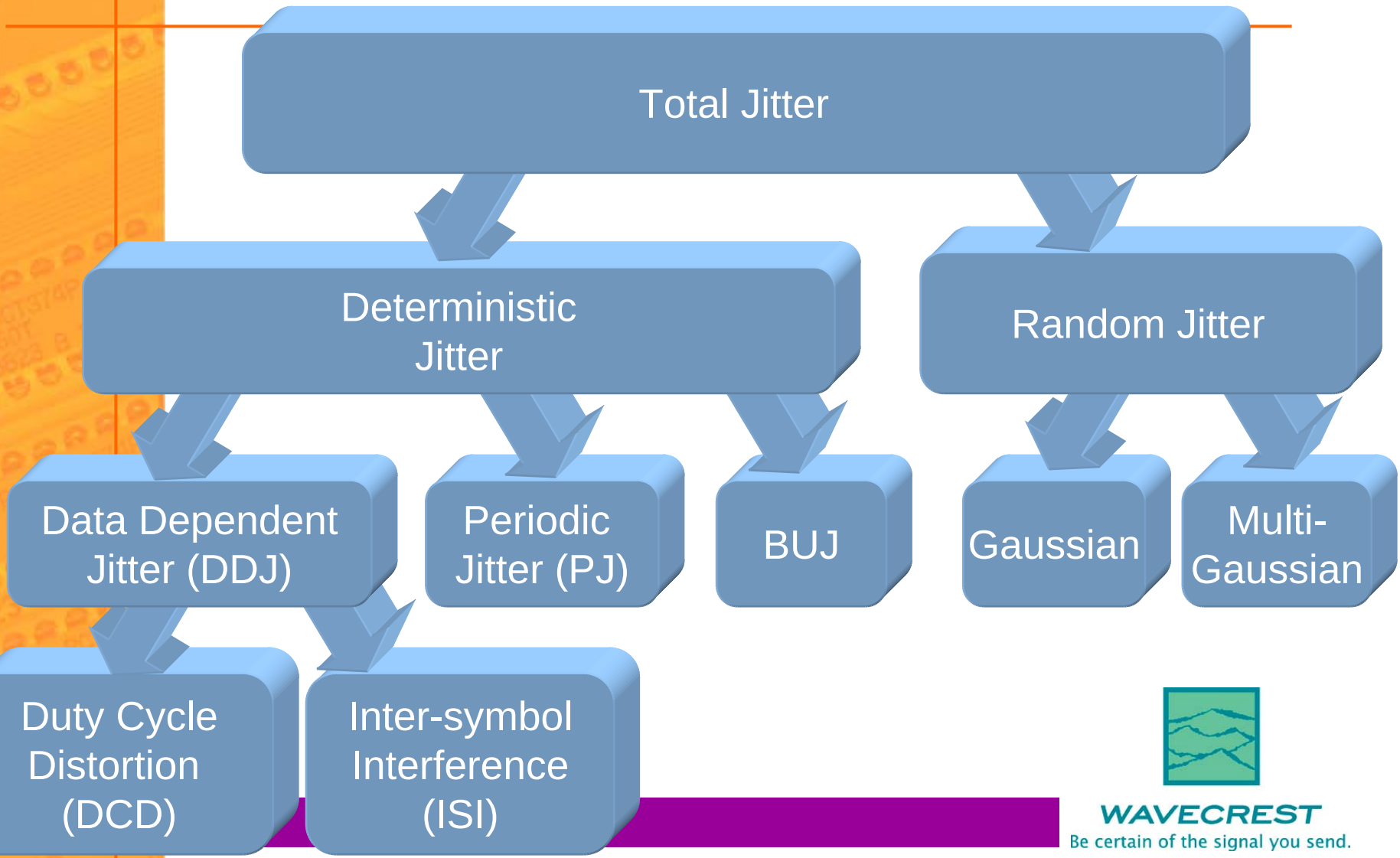
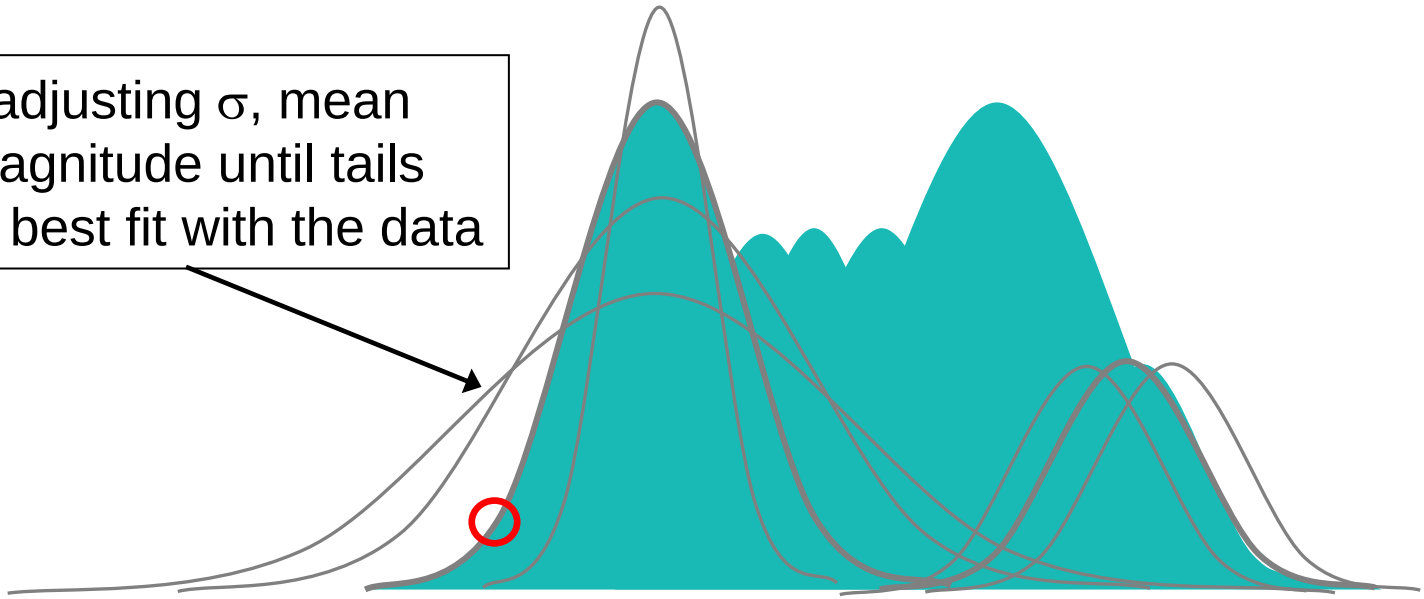
Jitter Terminology Review



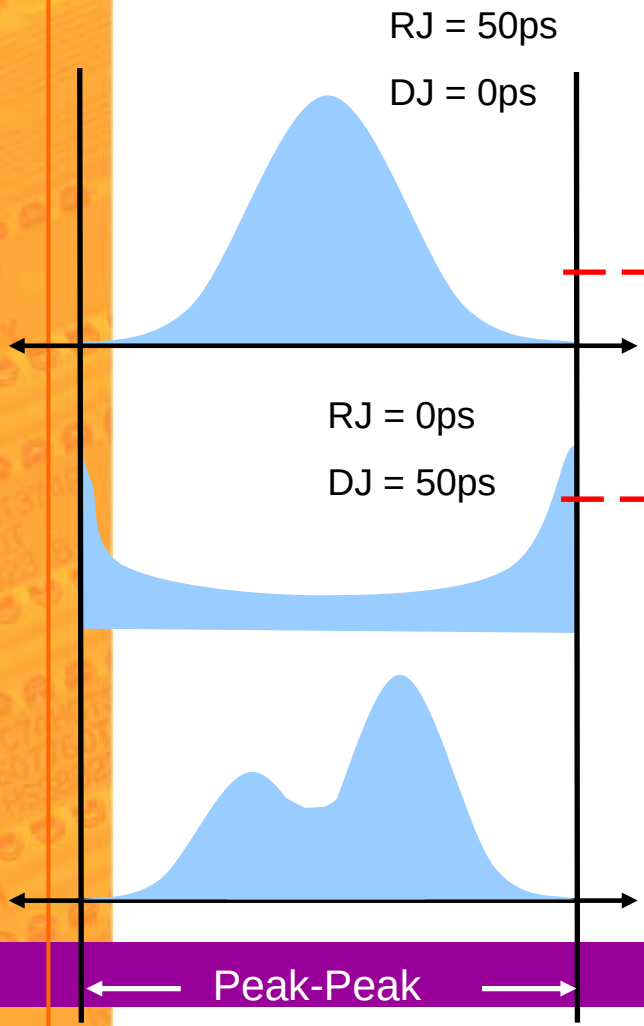
Measuring Random Jitter

Fit Gaussian tails to left and right side of distribution, TailFit™

Keep adjusting σ, mean and magnitude until tails obtain best fit with the data



Why Peak-to-Peak is a Poor Metric



Example:

	TJ@100 samples	TJ@10,000 samples
RJ = 50ps, DJ = 0ps	50ps	200ps
RJ = 0ps, DJ = 50ps	50ps	50ps

- Peak-to-Peak uses the first and last data point and ignores the rest of the data

Peak-to-Peak is a poor metric for determining system performance!

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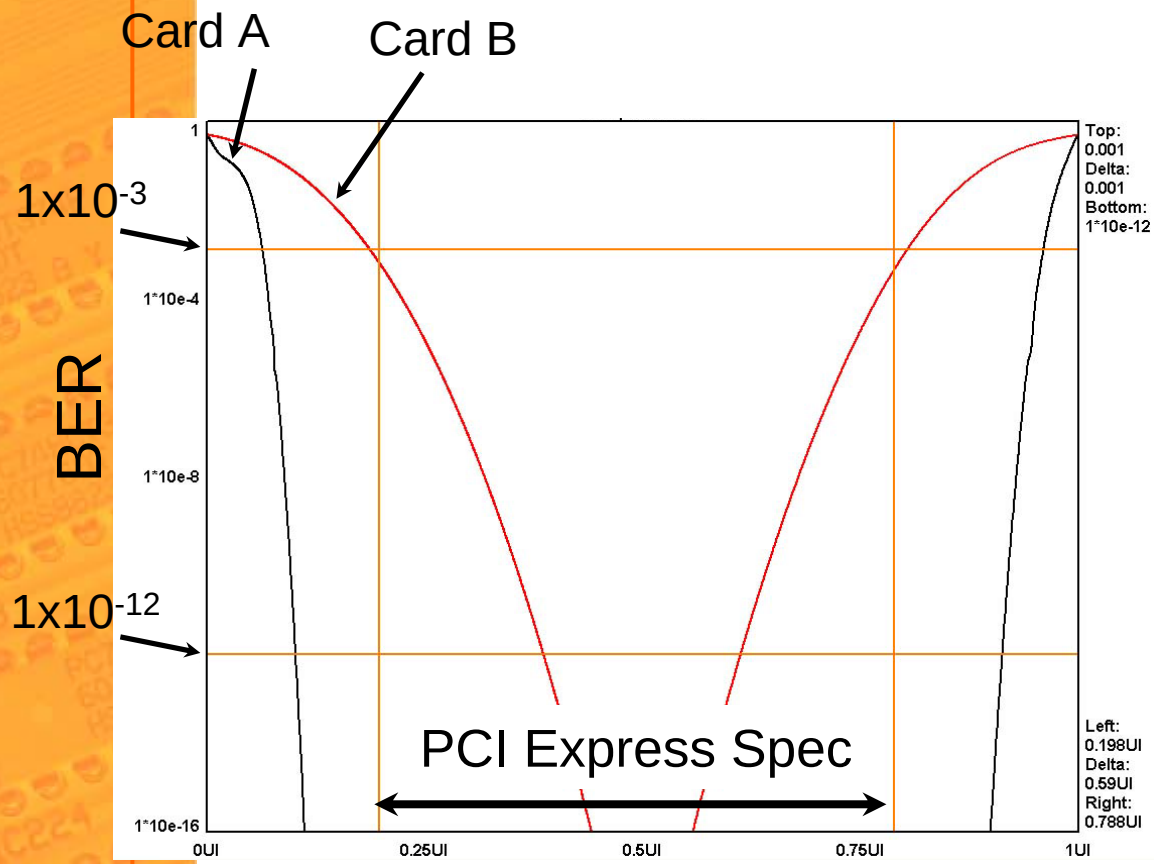
Why are Statistics So Important?

Because with insufficient statistics you can pass BAD parts



- Add-in card example
- Card B had link training problems
- Sample size of 1000 from software compliance measurement on a real-time oscilloscope-**both parts PASS**
- Comprehensive test to actual BER specification indicates part B **FAILS**

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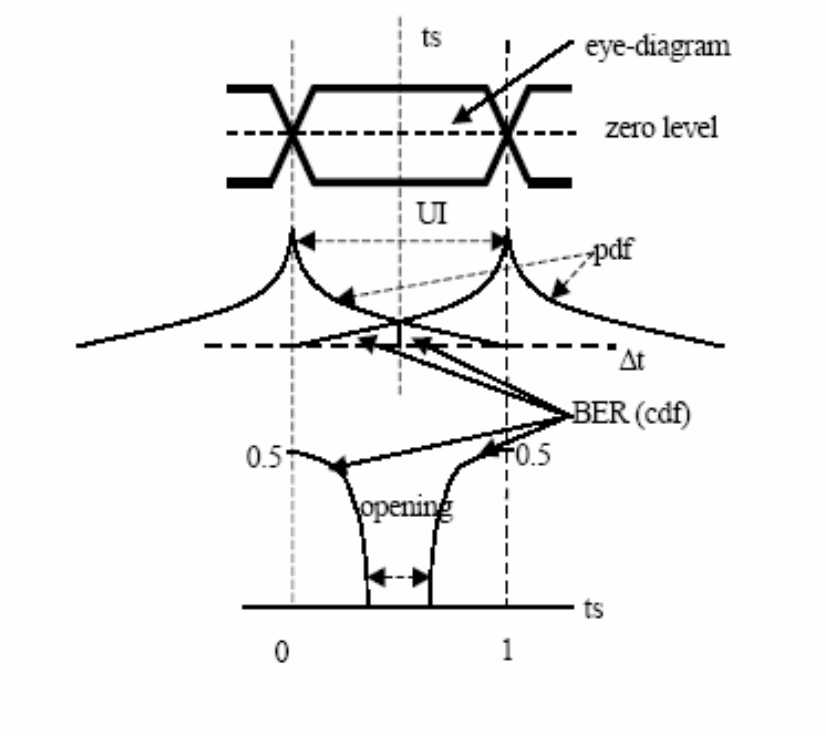
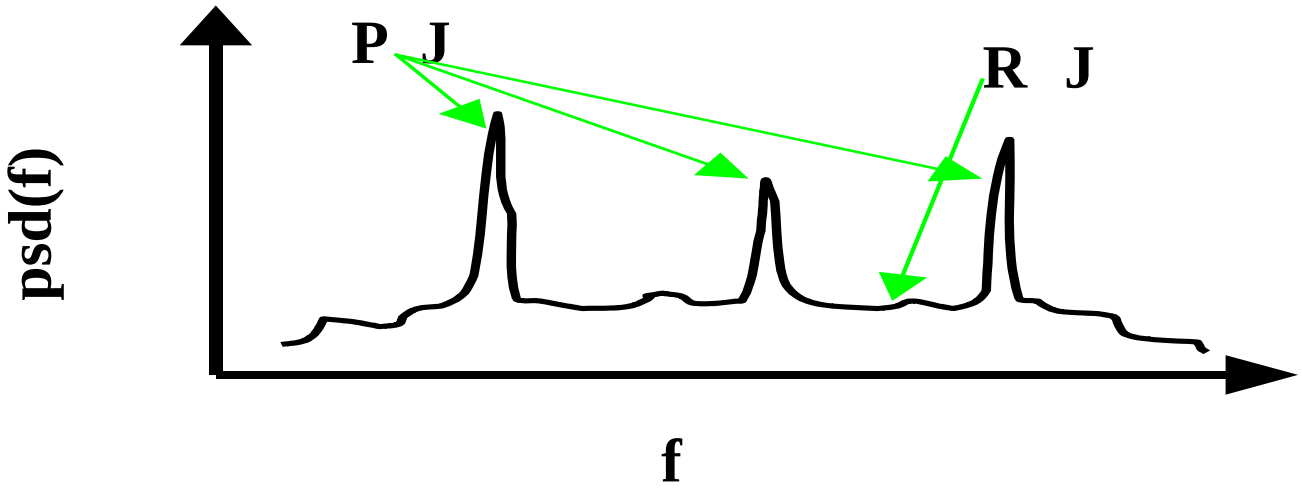
PDF, CDF, and Eye-Diagram In One View

- Relationship of Eye Diagram, TJ PDF and CDF



$$BER(t_s) = \frac{1}{2}[\int_{t_s}^{\infty} f_{TOT}(t)dt + \int_{-\infty}^{t_s} f_{TOT}(t - UI)dt]$$

Jitter Separation in Frequency-Domain



Variance/Autocorrelation method for

- RJ PSD
- PJ PSD
- DDJ (DJ without PJ and BUJ) PSD

II: Jitter Analysis and Test in Serial Data Communications

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Definitions

Understanding Jitter Bit Error Rate Statistics

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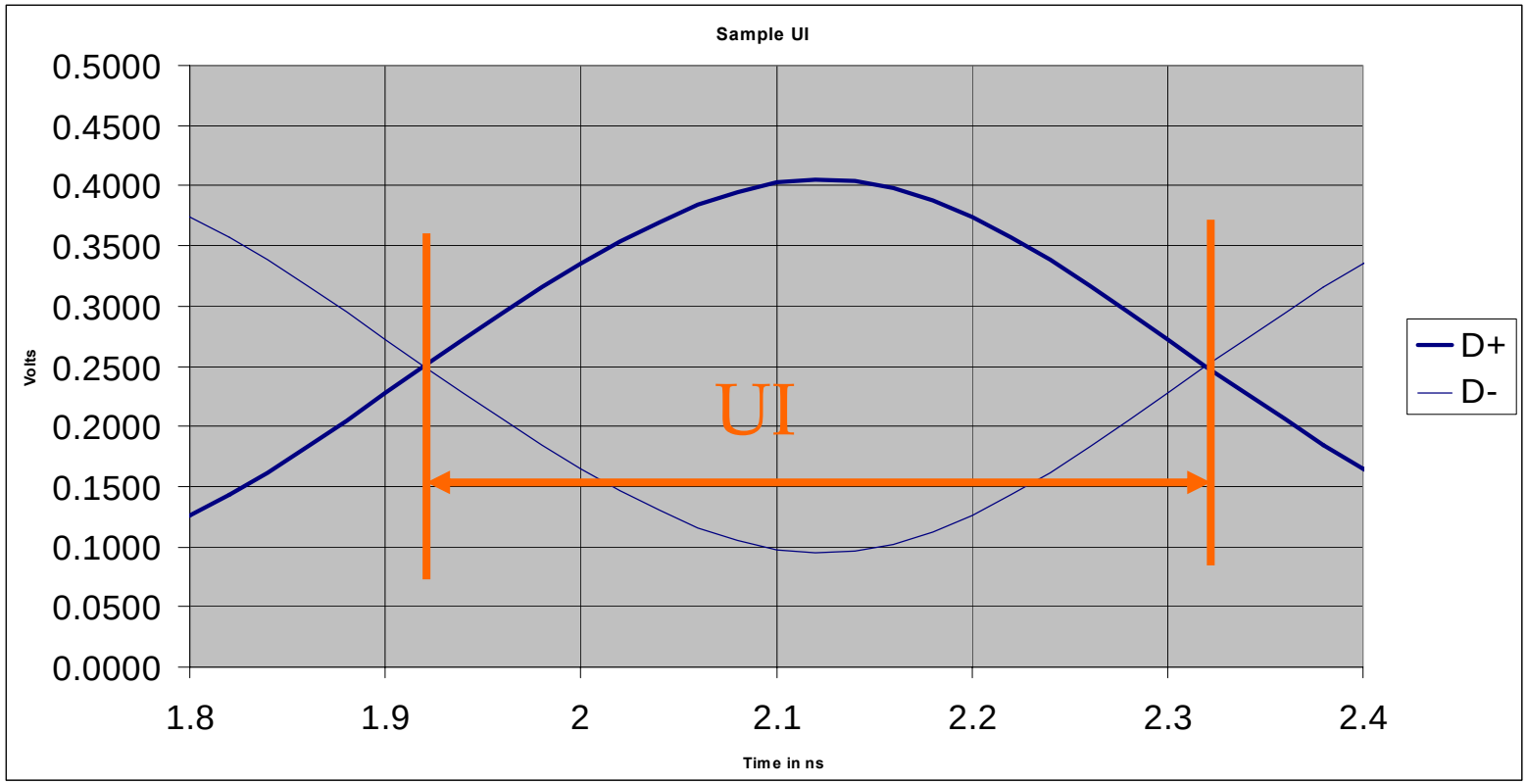
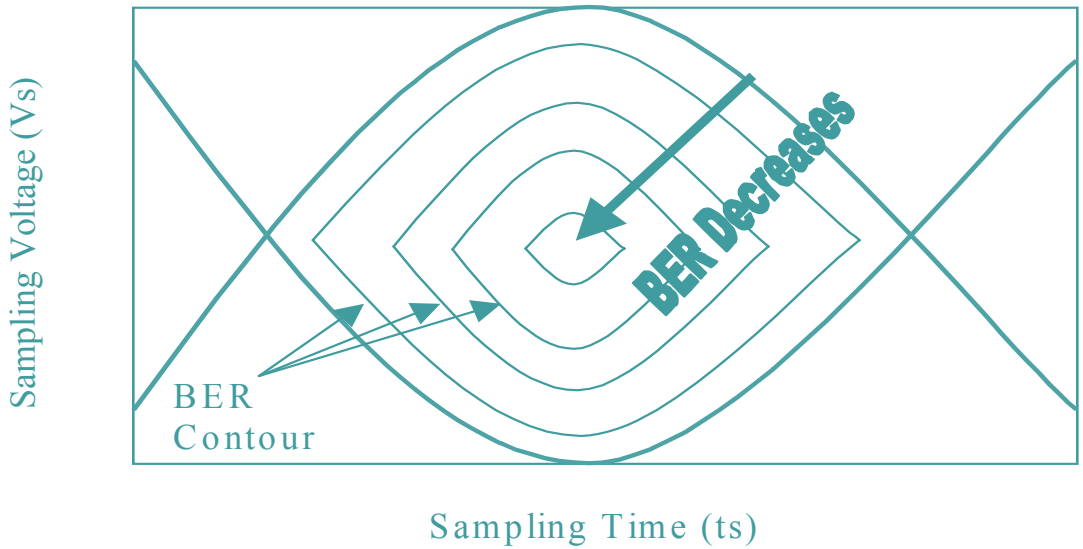
Bit Cell



- Bit UI boundary is between two crossing points of D+ and D- of a clock pattern

BER Contour



- Lowest BER at the center of the contour
- Total Jitter is defined at BER = 10^{-12} for PCI Express Base Specification

Types of Jitter Quantification

- Should I perform a Phase (Accumulated Jitter), Period or Cycle-to-Cycle Jitter measurement?
- Why do these measurements give different numbers for the same signal?
- Does the measurement emulate the device or system?

Phase, Period, and Cycle-to-Cycle Jitter

Units Of Jitter

- Time and Phase are used interchangeably to quantify jitter
- Difference in time is:

$$\Delta T = T_{ideal} - T_{measured}$$

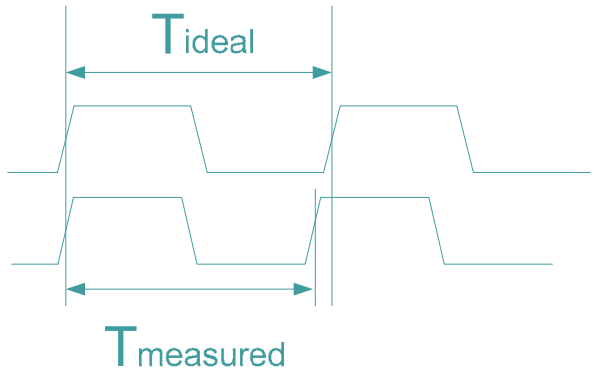
- Difference in phase is:

$$\Delta Phase = 2\pi - 2\pi \frac{T_{measured}}{T_{ideal}}$$

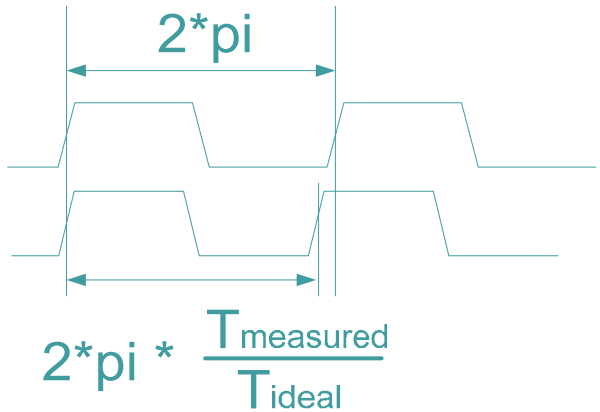
- The conversion is simply:

$$\Delta Phase = \frac{\Delta T}{T_{ideal}} * 2\pi$$

Time:

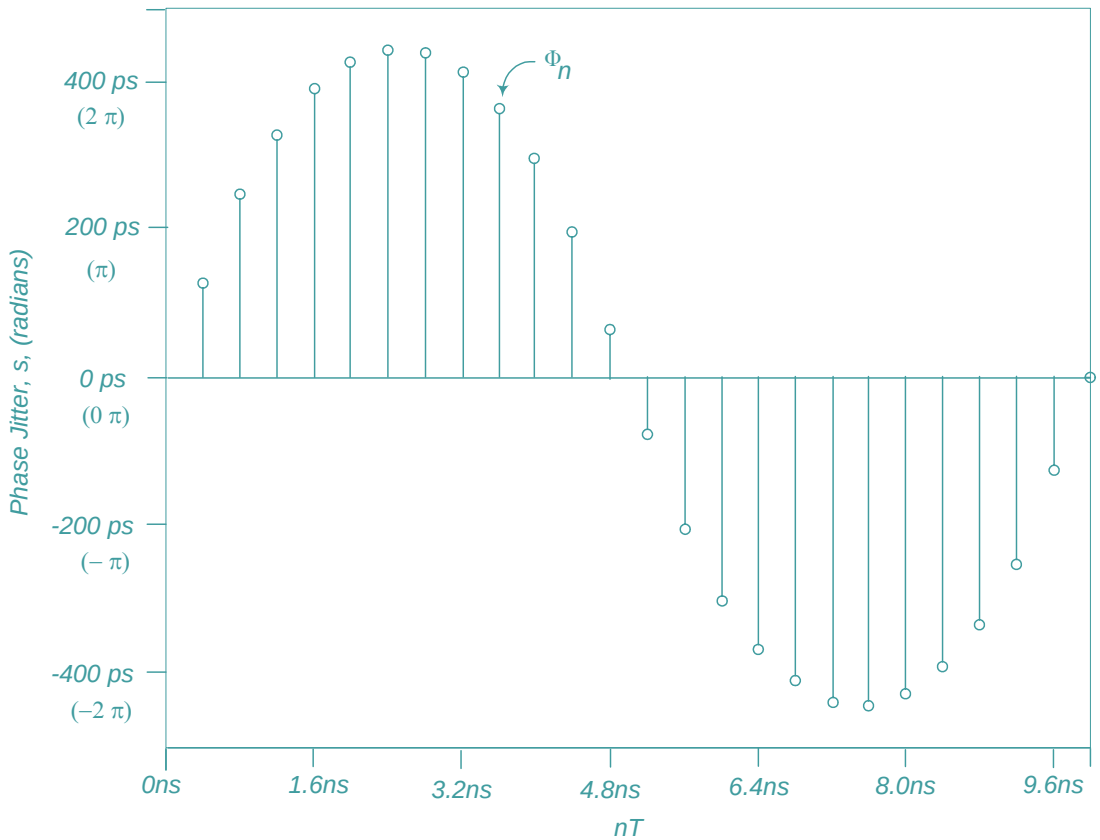


Phase:



Phase Jitter (Φ)

- Also known accumulated jitter $\Phi_n = t_n - nT, \quad n = 1, 2, \ldots, \infty$

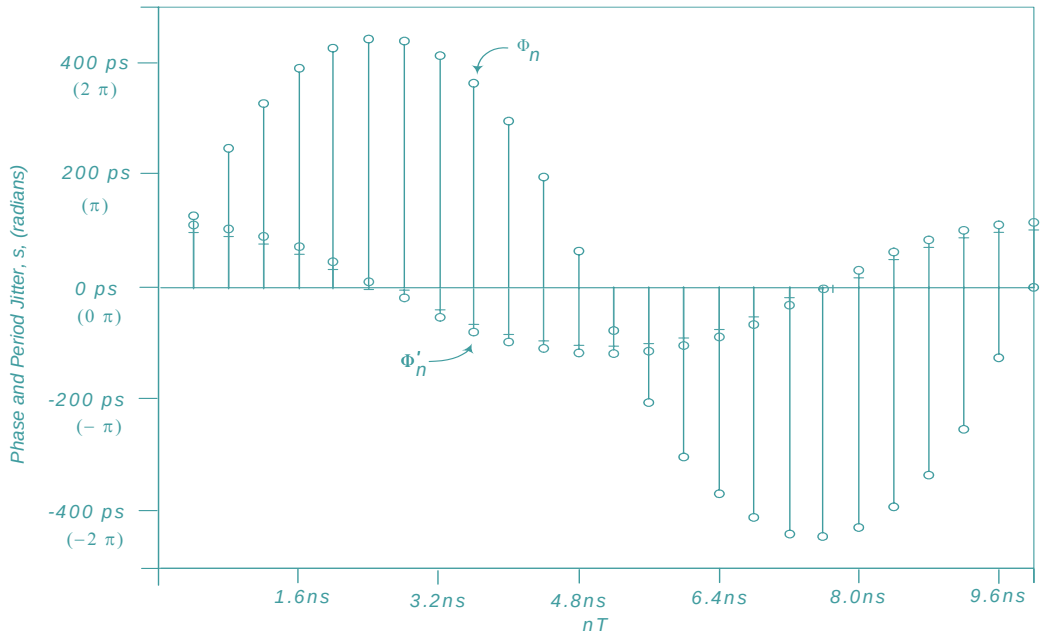


Period Jitter (Φ')

- Period Jitter
  - The period Jitter (Φ') is the difference between the measured period and the ideal period
- Also is

$$\Phi'_n = (t_n - t_{n-1}) - T, \quad n = 1, 2, \ldots, N$$

$$\Phi'_n = \Phi_n - \Phi_{n-1}$$



Cycle-to-Cycle Jitter (Φ')

- Cycle-to-Cycle
  - The difference between consecutive bit periods

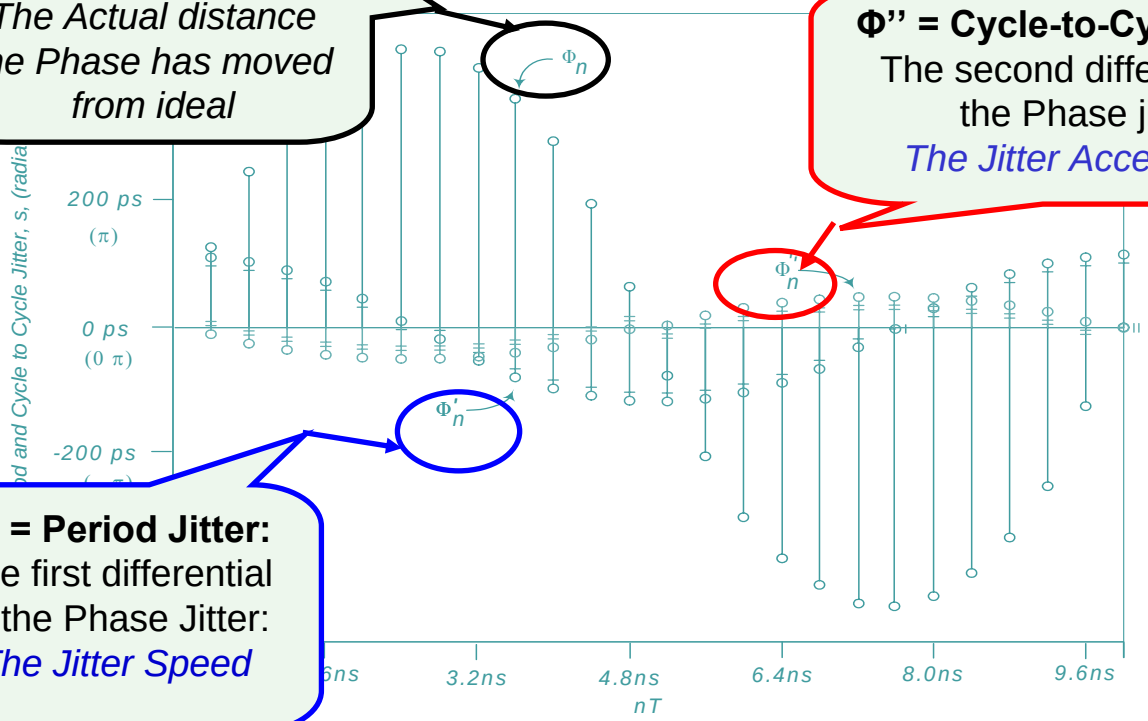
- Also is

$$\Phi''_n = (t_n - t_{n-1}) - (t_{n-1} - t_{n-2}), \quad n = 1, 2, \ldots, N$$

$$\Phi''_n = \Phi'_n - \Phi'_{n-1}, \quad n = 1, 2, \ldots, N$$

Φ = Phase Jitter:
The Actual distance the Phase has moved from ideal

Φ'' = Cycle-to-Cycle Jitter:
The second differential of the Phase jitter:
The Jitter Acceleration



Φ' = Period Jitter:
The first differential of the Phase Jitter:
The Jitter Speed

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Interrelationship

- Phase Jitter → Period Jitter → Cycle-to-cycle

$$\Phi''_n = (\Phi'_n)' = (\Phi_n)''$$

- Cycle-to-cycle → Period Jitter → Phase Jitter

$$\Phi_n = \int \Phi'_n = \iint \Phi''_n$$

- Different representations of a same physical phenomena
- Analogy to Newton's
  position <->velocity<->acceleration
  relationships

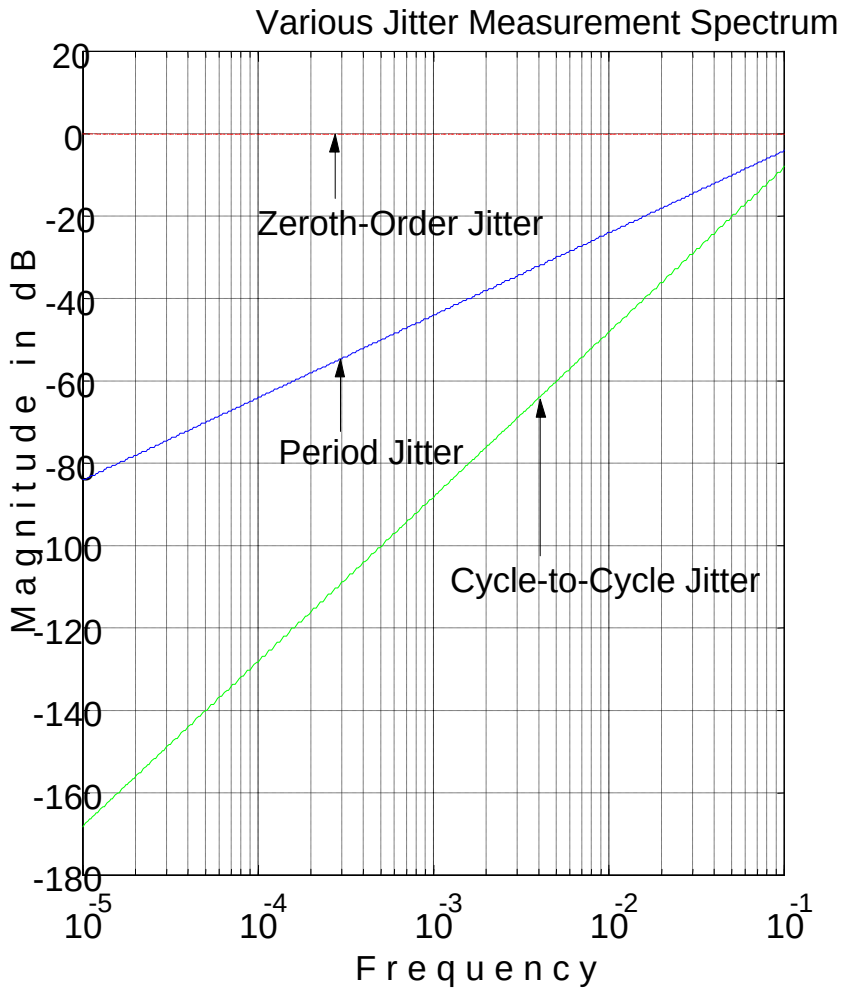
Interrelationship in Frequency Domain

$$If\ (\Phi_{phase}(f) = c)$$

$$Then$$

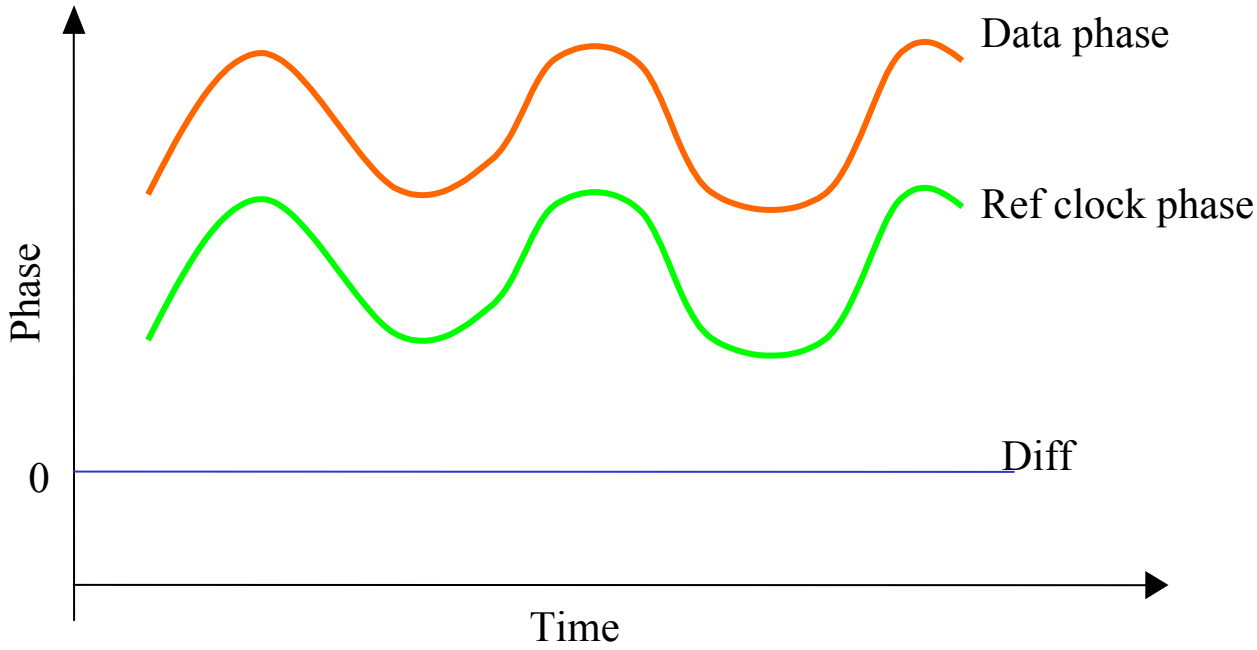
$$\Phi_{period}(f) \propto f \bullet c$$

$$\Phi_{cycle-cycle}(f) \propto f^2 \bullet c$$



Phase Jitter Measurement and Reference Clock Used

- Calculating Phase Jitter against a warped clock (or recovered clock) reduces the amount of Phase Jitter calculated
- The amount of warping depends on the recovered clock's transfer function of the receiver



Eye Closure/Total Jitter Modeling

- Given a clock and data signal

$$V_{Clk}(t) = V_{0Clk}[\omega_{Clk}t + P_{Clk}(t)]$$

$$V_{Data}(t) = V_{0Data}[\omega_{Data}t + P_{Data}(t)]$$

- Eye closure $\Delta P(t)$ is the difference in the phase between the clock and the data given by

$$\Delta P(t) = | P_{clk}(t) - P_{data}(t) |$$

- ***Eye closure directly depends on the jitter transfer function of the receiver***

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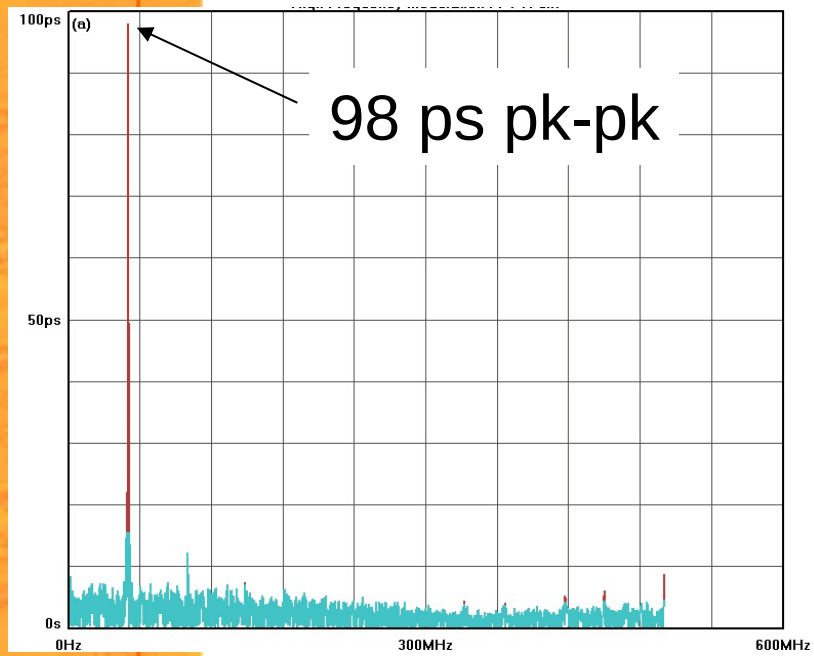
Types of Jitter Measure

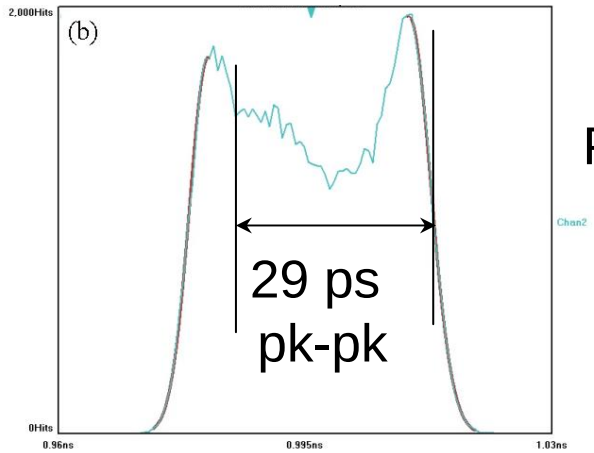
- Each type of measurement has a different effect on your results
- Use the measurement that most represents how the signal you are testing will actually be used
  - If designing a PLL, use Phase Jitter because the output is proportional to the phase error of the reference and output signal
  - For diagnosing modulation or crosstalk, Phase and/or Period Jitter is appropriate
  - Applications for Cycle-to-Cycle????

Real-World Example

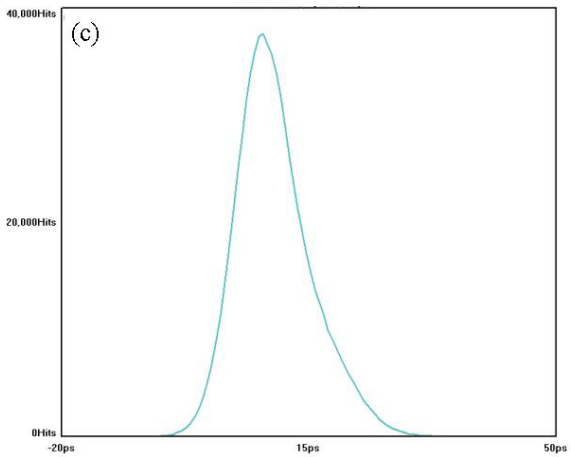
- 1 GHz clock with a 50 MHz modulation



Accumulated Jitter



Period Jitter



Cycle-to-Cycle Jitter

LTI Systems

An Overview of Linear Time-Invariant (LTI) System and Transfer Functions

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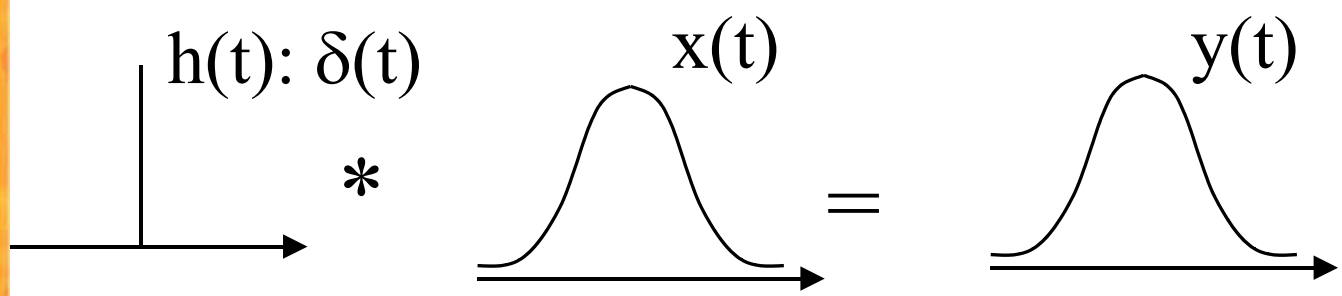
LTI System in Time-Domain

- An output signal y(t) equals to the input signal convolves with the impulse response h(t)

$$y(t) = \int_{-\infty}^{\infty} x(\tau)h(t-\tau)d\tau$$



- Phase jitter is modeled as continuous signal

LTI System in S-Domain

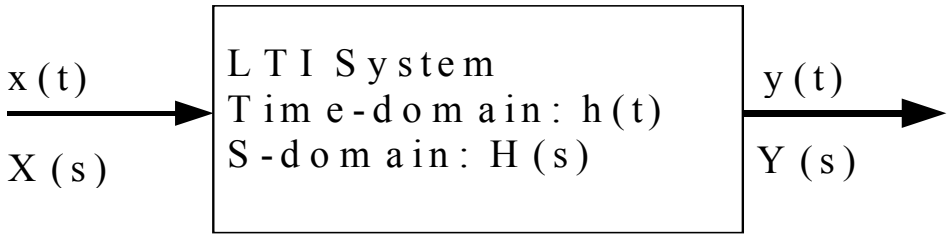
- S-domain function is obtained via Laplace transformation

$$Y(s) = X(s)H(s)$$

$$y(t) = \text{Laplace}^{-1}\,(Y(s))$$

- Complex frequency **s** can be related to the real frequency ω through **s** = jω, as done in the models

LTI System Summary



$$y(t) = h(t) * x(t) = \int_{-\infty}^{\infty} x(\tau)h(t-\tau)d\tau$$

$$Y(s) = H(s)X(s)$$

$$H(s) = \int_{-\infty}^{\infty} h(t)e^{-st}dt$$

Jitter Transfer Function

The Jitter “Seen” by the System

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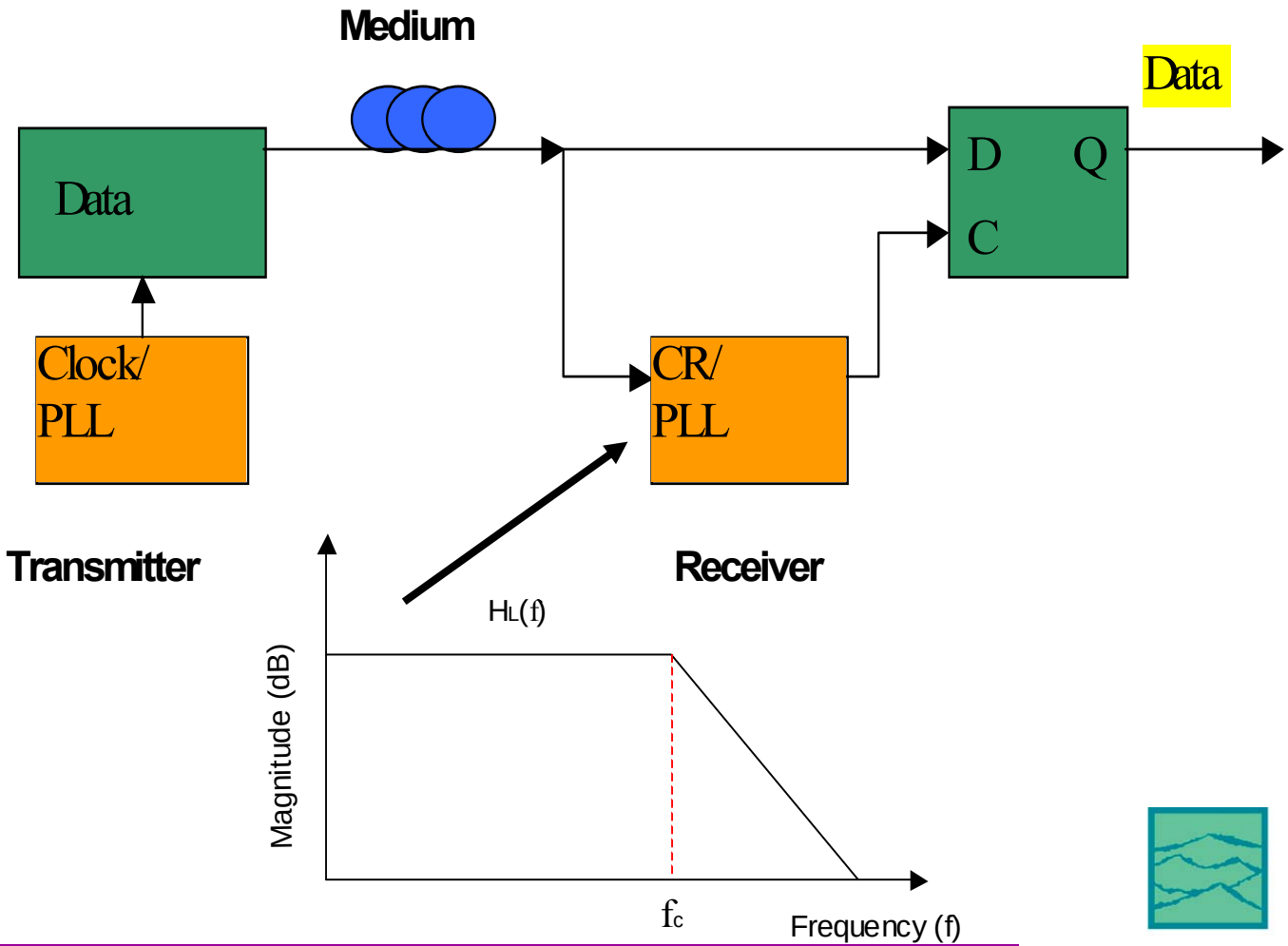
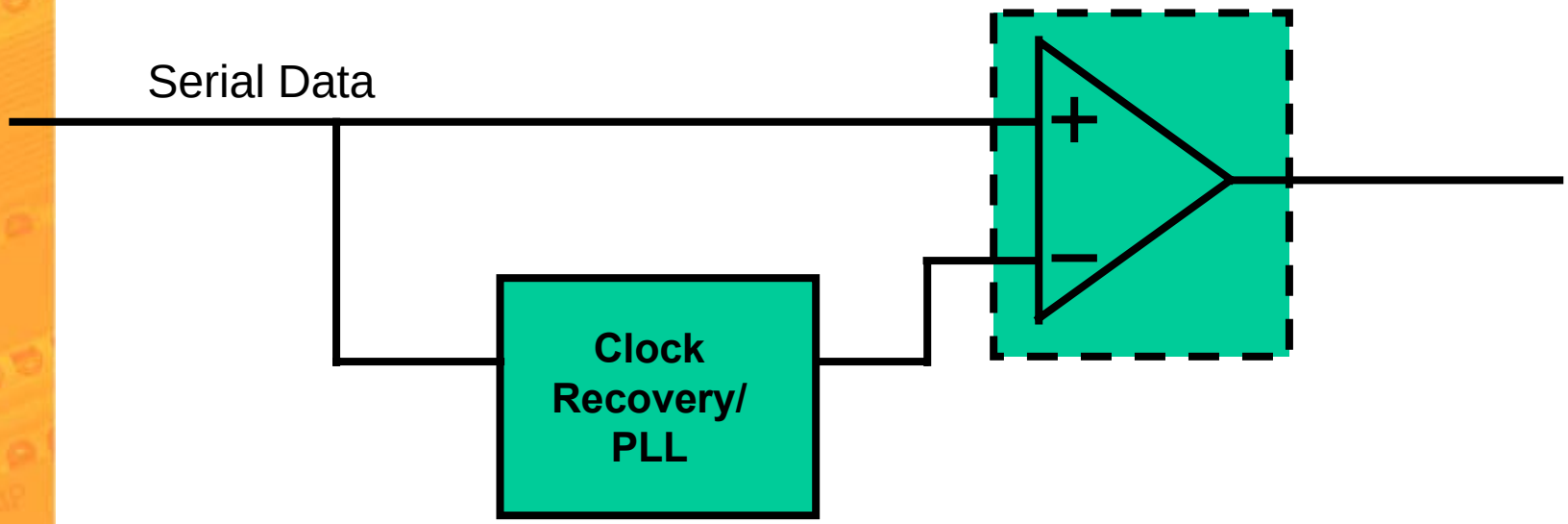
A Serial Data Communication System



Receiver Jitter Transfer Function



Receiver sees a “Difference” Function

- The difference of the position of the reference clock edge to the date edge

What Does a Difference Function Mean?

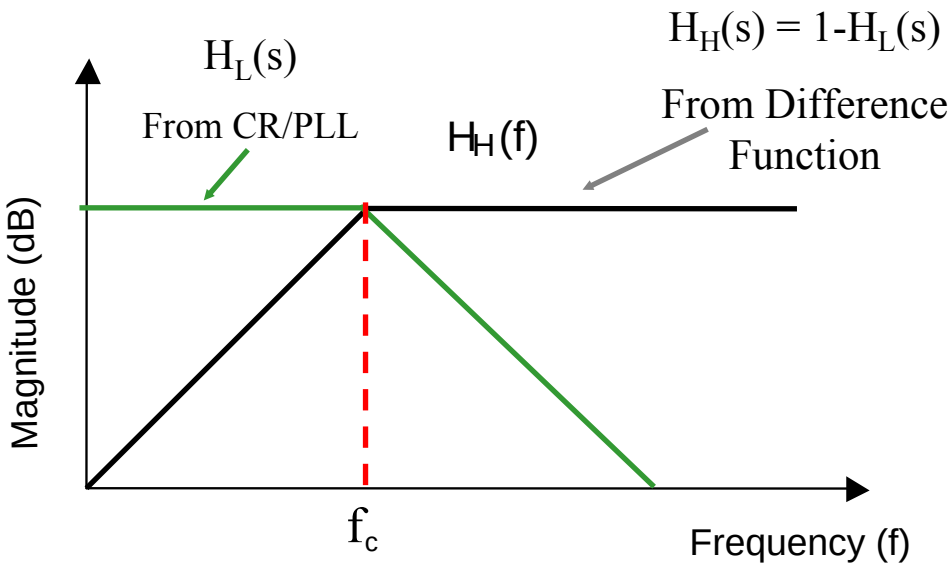
- Jitter is referenced to a recovered bit clock
- Receiver has a jitter transfer function
- “Intrinsic” jitter is not the jitter “seen” by the receiver
- BER of the system should be estimated based on jitter “seen” by the receiver

Jitter Transfer Function

$$\frac{\theta_e}{\theta_i} = 1 - H_L(s)$$

$$= H_H(s)$$

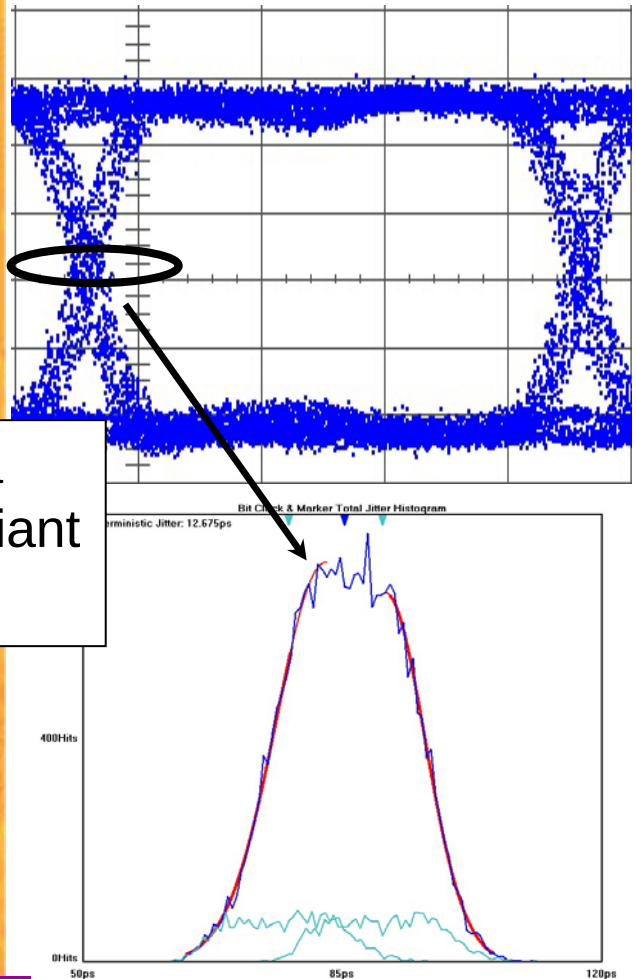
A First Order Jitter Transfer Function



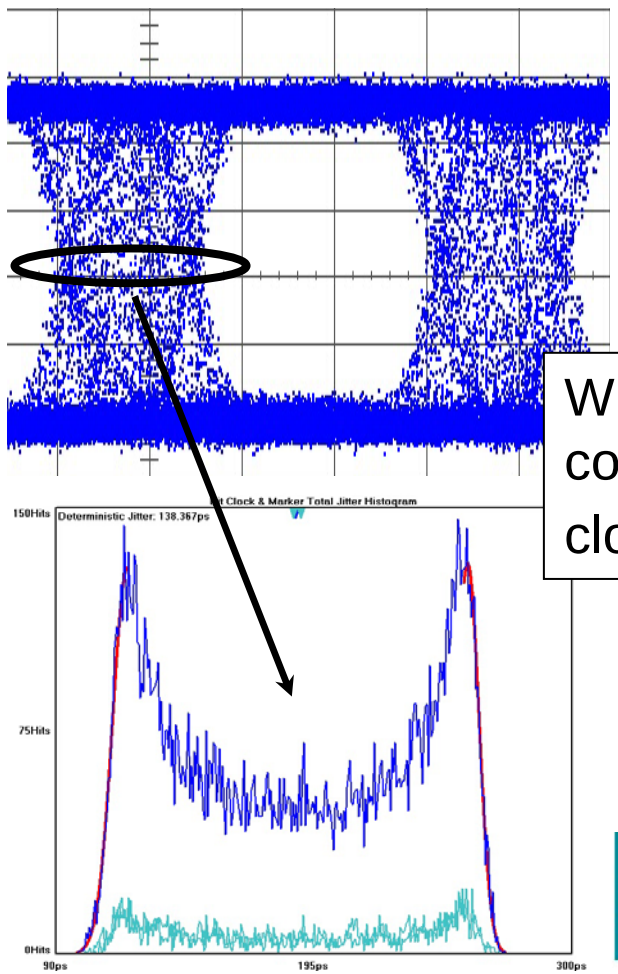
Frequency Response "Corner Frequency"

- Frequency response "corner" frequency fc is determined by clock recovery subsystem
- Many serial data communication standards adopted the "1667" rule, e.g., FC, GBE, SONET
  - fc = Databaud/1667
- For PCI Express version 1.1, this corner frequency fc is 2.5 Gb/s divided by 1667 or 1.5 MHz

Effect of Clock Recovery On Your Measurements cont.



With a compliant clock



Without a compliant clock

III: Link Architecture and Jitter

References

1. Li, Martwick,Talbot, Wilstrup, 2004, ITC paper on PCI Express Jitter, ITC Proceedings
2. PCI Express Jitter white paper, 2004: http://www.pcisig.com/specifications/pciexpress/technical_library#jitter
3. Li, 2005, ITC paper on Jitter, Noise, and BER test, ITC Proceedings

3.1 System Architectures and Models

System Clock Recovery, Jitter and Transfer Function models

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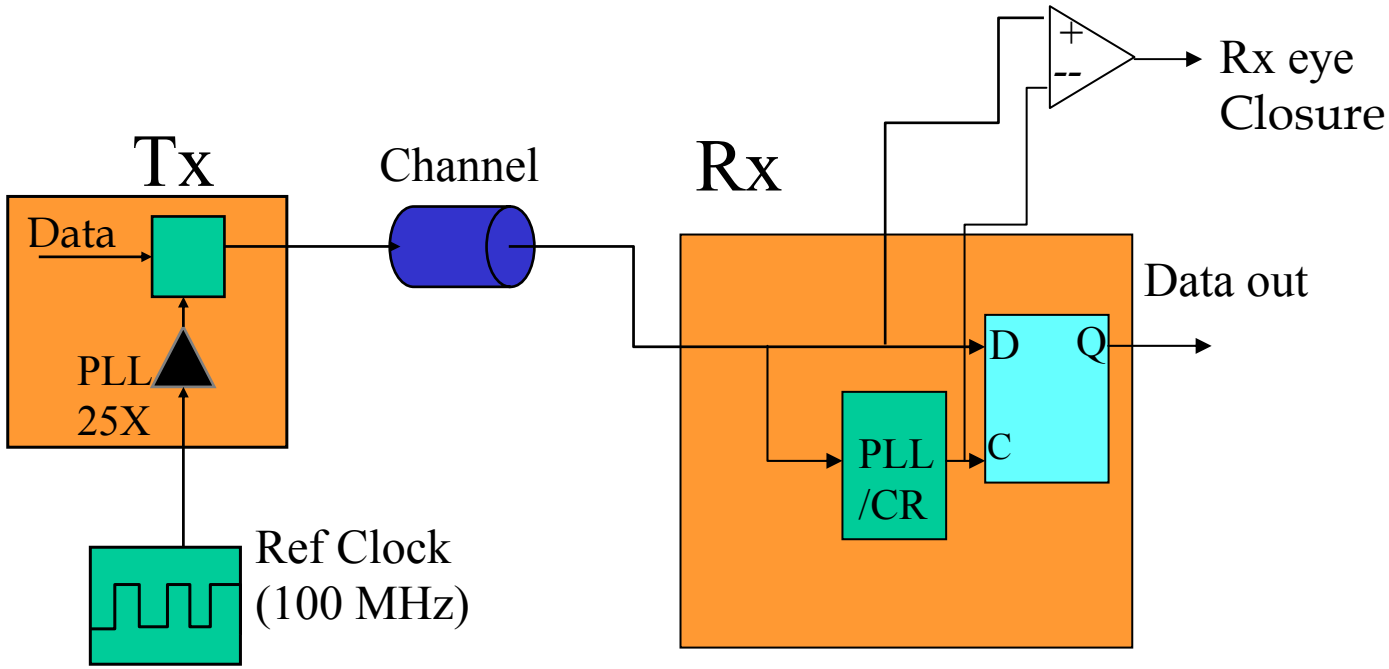
Data Recovery Circuits (DRC)

- Receiver Data Recovery is the essence of the system
- Traditional serial communication uses a PLL-based Data Recovery
- Recent computer Gbps links (e.g., PCIe) allow a less expensive digital-based Data Recovery Circuit
  - Using Phase Interpolator (PI), Over-Sampling (OS) or Digital Controlled delay line
  - Majority implemented DRCs are PIs

PLL Based DRC (e.g., FC, GBE, PCIe)

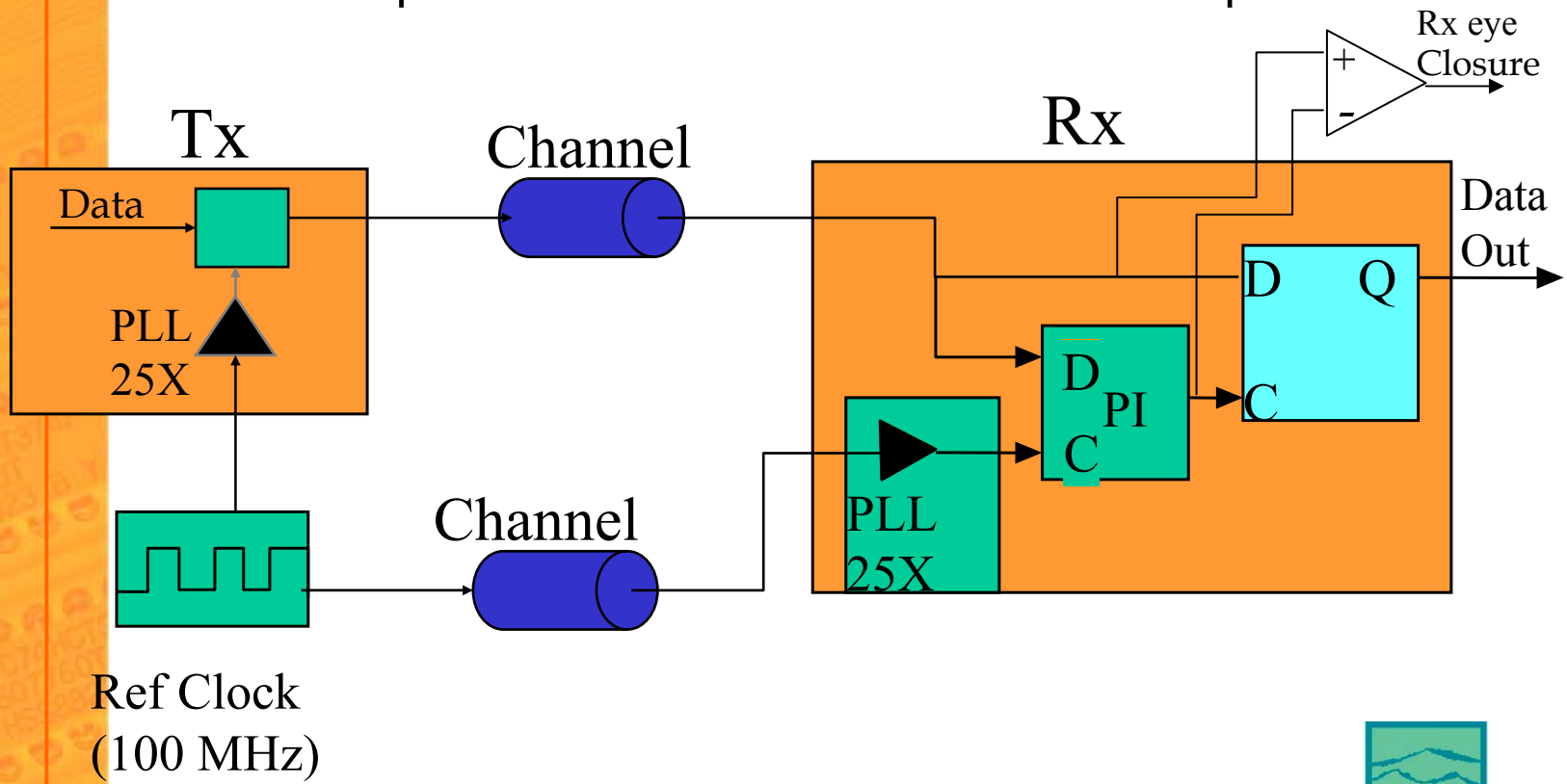
- The system reference clock is not used by DRC
- The Rx PLL needs to track the transmitter's jitter output



Eye-closure / total jitter system model

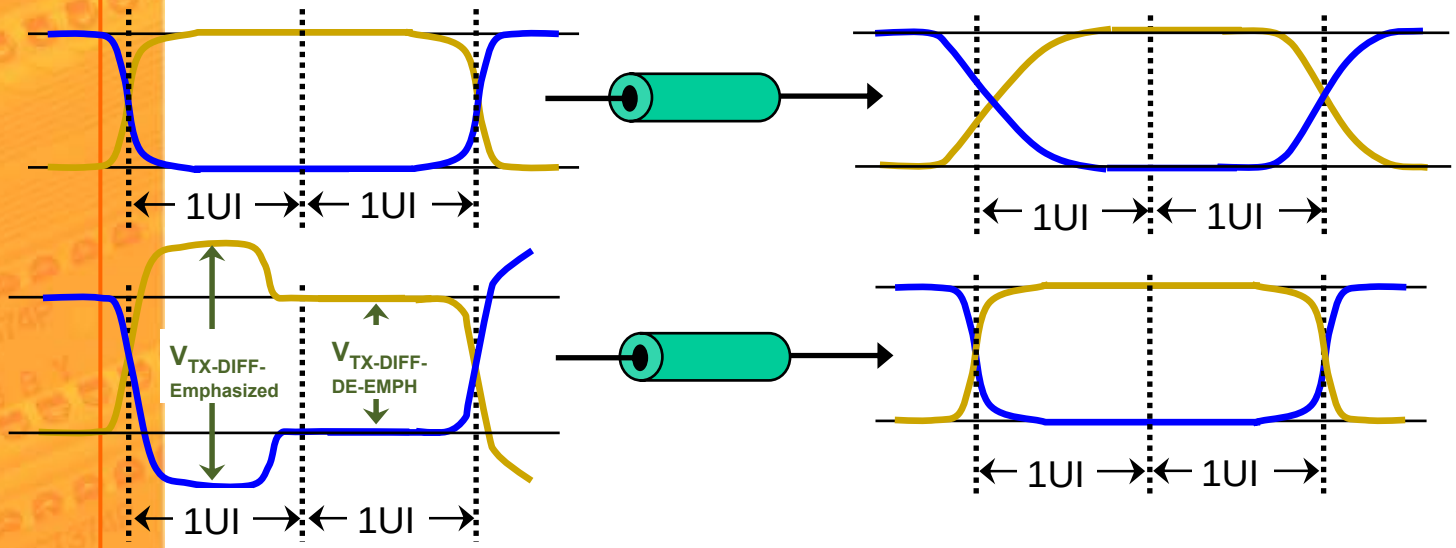
Digital PI Based DRC (e.g., PCIe, FB DIMM)

- Both Tx and Rx use the reference clock
- Phase relationship between reference clock and data path matters



Eye-closure / total jitter system model

De-Emphasis



Channel Slows Edges: Bit window is reduced: Data Dependent Jitter (DDJ)

De-Emphasis Compensates: Exaggerated edges at TX result in better Bit window at RX

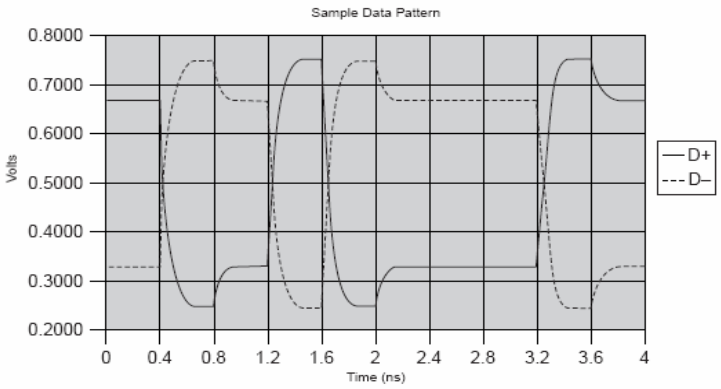


Figure 4-41~~4-21~~: Sample Transmitted Waveform Showing -3.5 dB De-emphasis Around a 0.5 V Common Mode Voltage

De-Emphasis tries to compensate for DDJ of the Channel

Phase /Jitter Transfer Function for a PLL

- The input signal to a PLL is

$$V_{in}(t) = A_{in}\sin\left(\omega_{in}t + P_{in}(t)\right)$$

where $P_{in}(t)$ is the input phase signal and is the state variable of the PLL

- The output from a PLL is

$$V_{out}(t) = A_{out}\sin\left(\omega_{out}t + P_{out}(t)\right)$$

where $P_{out}(t)$ is the output phase.

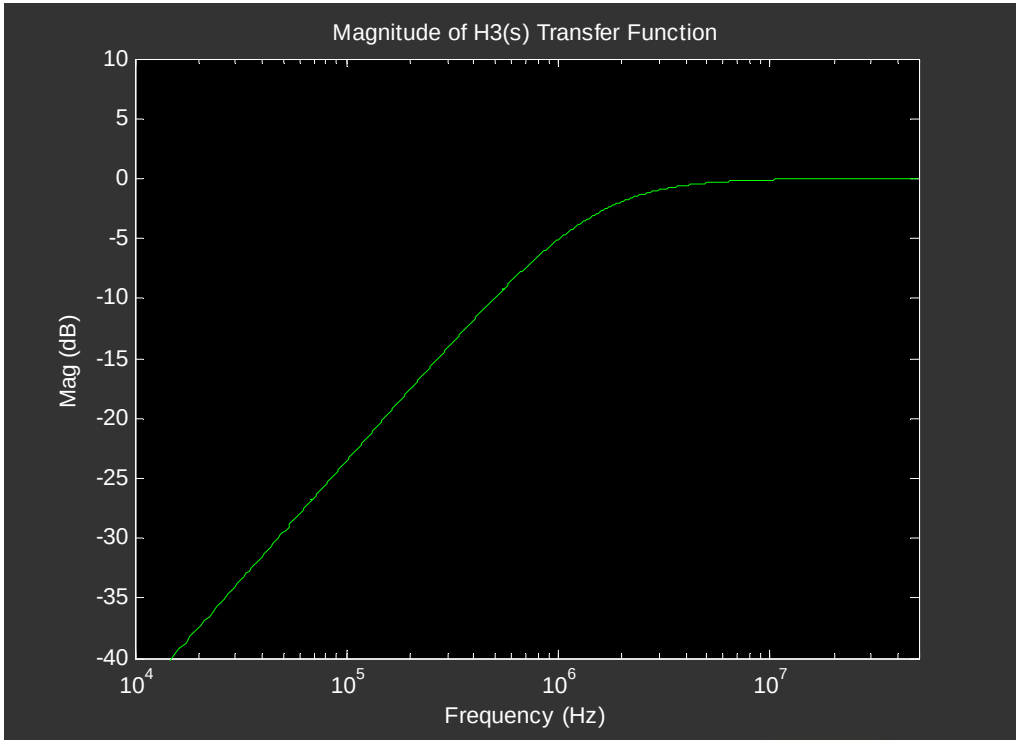
- The PLL has a phase transfer response h(t)/H(s), they satisfy

$$P_{out}(t) = h(t) * P_{in}(t) \quad P_{out}(s) = H(s)P_{in}(s)$$

Approximate Digital PI DRC Transfer Function

- The DRC Response is modeled by a first order F_3dB high pass(fc=1.5 MHz for PCIe)
  - This tracks the spread spectrum clock

$$H_3(s) = \frac{s}{s + \omega_3}$$

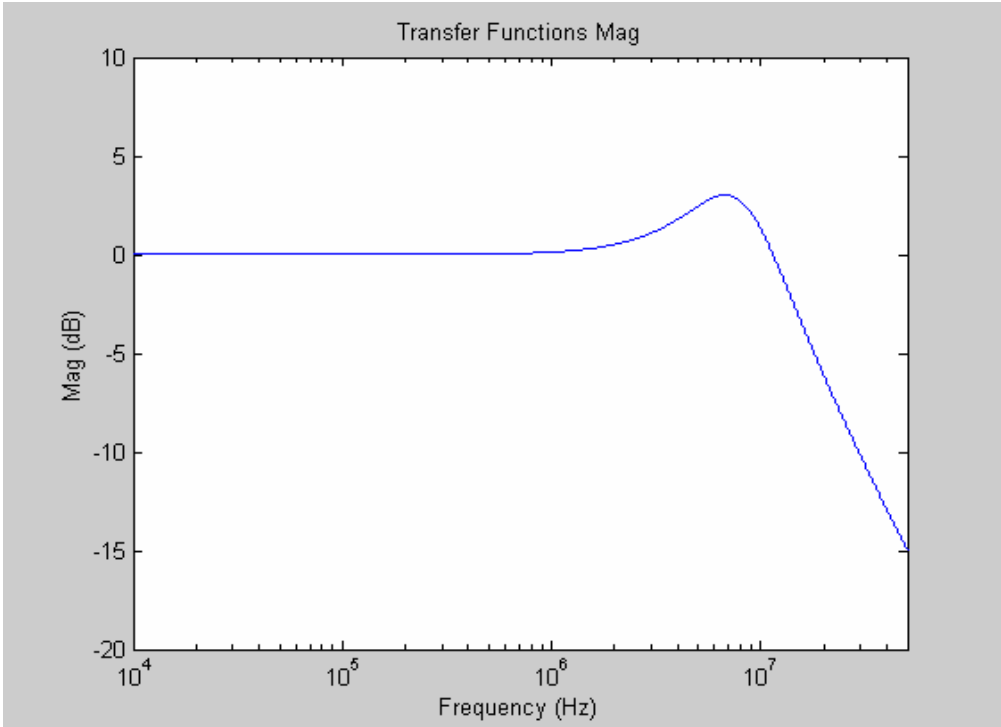


Model For a PLL Transfer Function

- Can be approximated with 2nd order transfer functions for Rx and Tx
- Some PLLs are 3rd order or higher. Additional poles are higher frequency and do not contribute significantly to the eye closure

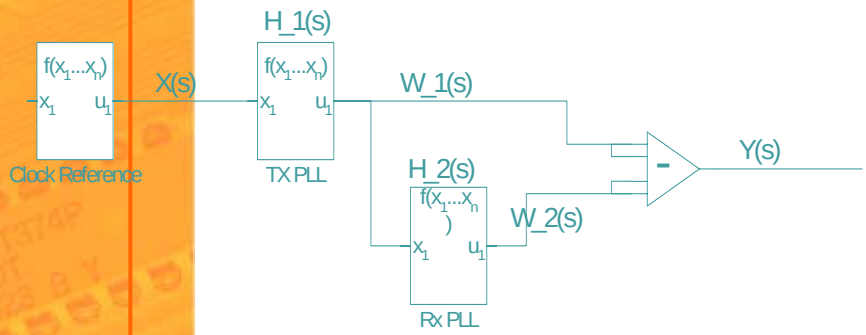
$$H1(s) = \frac{2s\zeta\omega_n + \omega_n^2}{s^2 + 2s\zeta\omega_n + \omega_n^2}$$

$$\omega_{3dB} = \omega_n \sqrt{1 + 2\zeta^2 + \sqrt{(1 + 2\zeta^2)^2 + 1}}$$



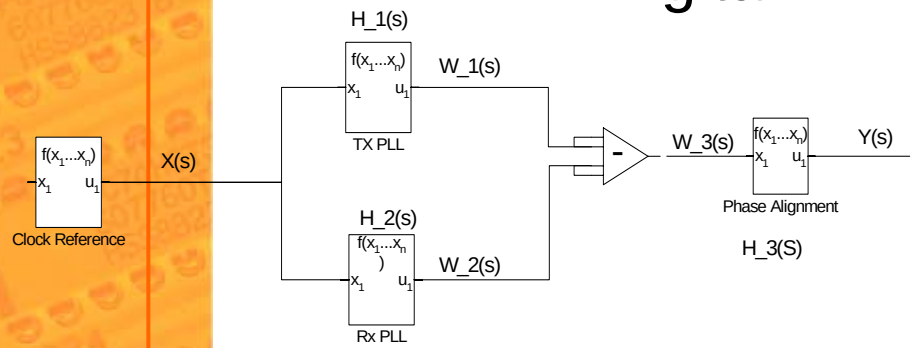
System Transfer Function Models

PLL Based DRC Model



$$H_t(s) = H_1(s)\left(1 - H_2(s)\right)$$

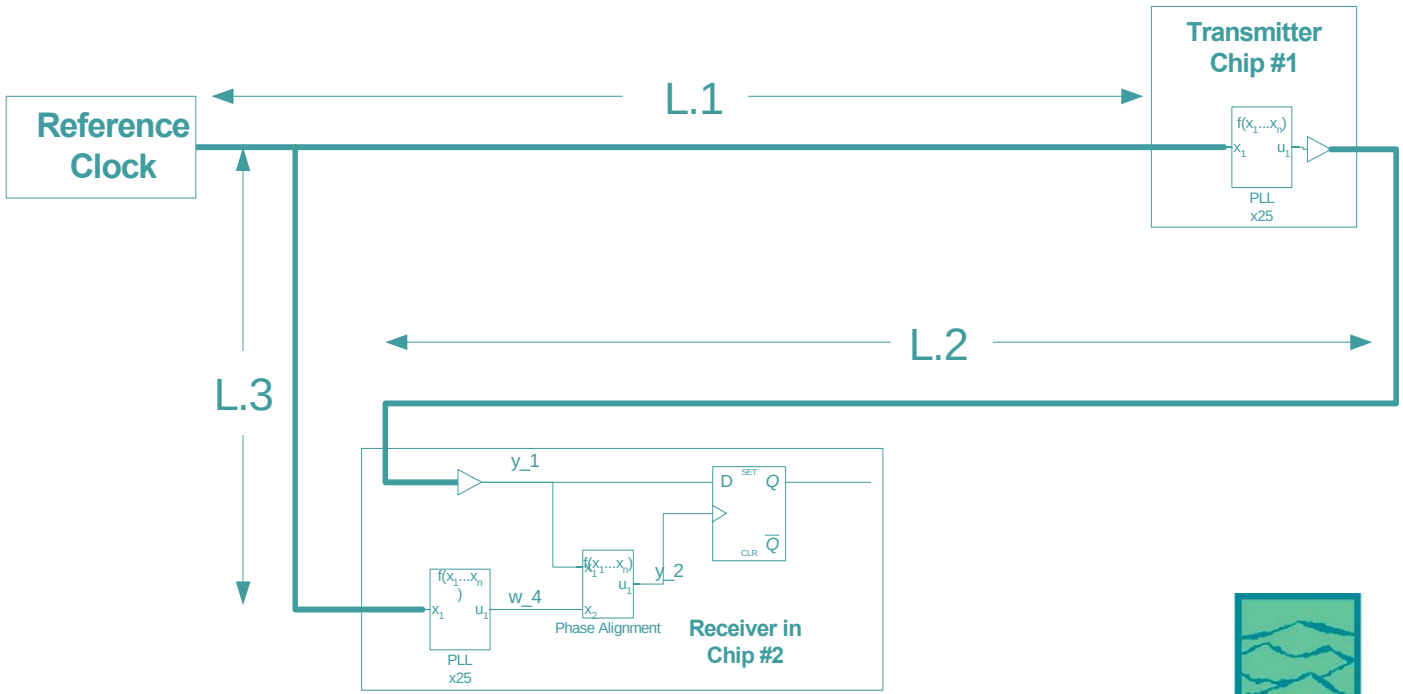
Digital PI DRC Model



$$H_t(s) = (H_1(s) - H_2(s))H_3(s)$$

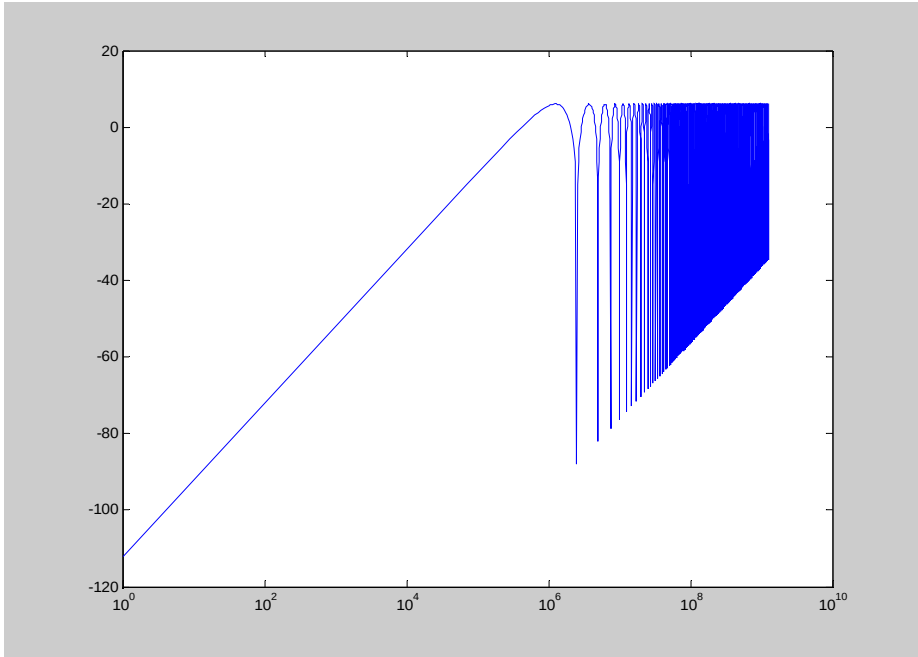
Delay Model

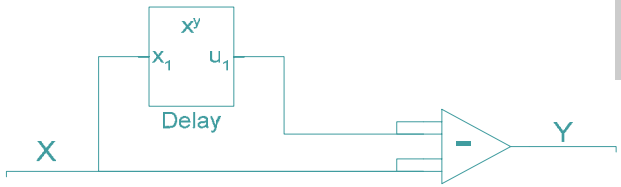
- Delay transfer function models into the system
  - The phase delay is given by (L1 + L2) – L3
  - This is modeled by exp(-s * t_delay)



Delay Transfer Function

- Example with 100 ns delay
- The transfer function has nulls at the delay period
- It has 6dB of gain at ½ intervals of the delay period
  - Doubles the effective jitter



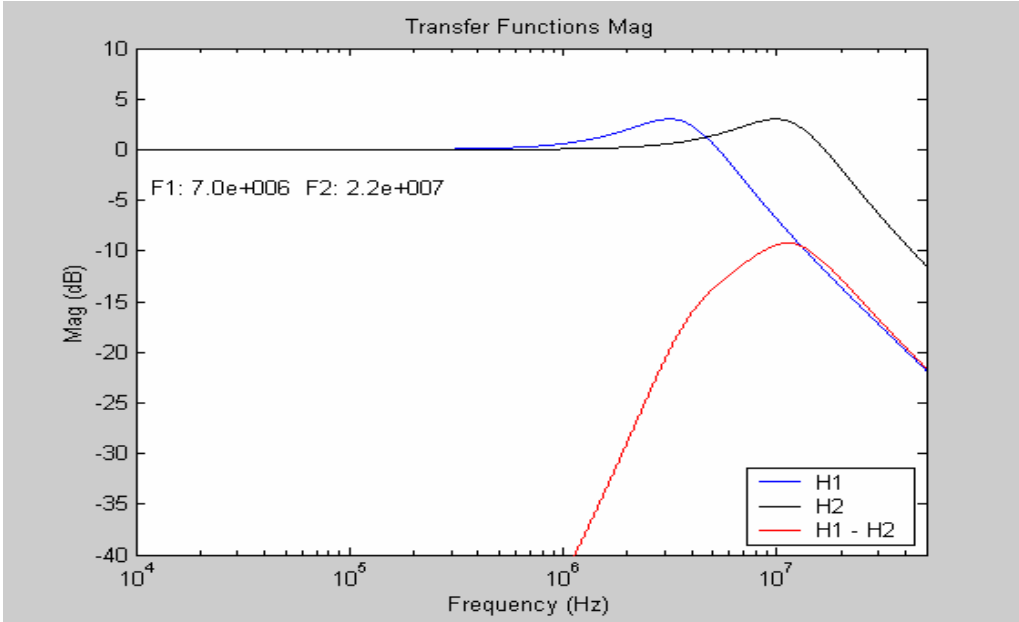


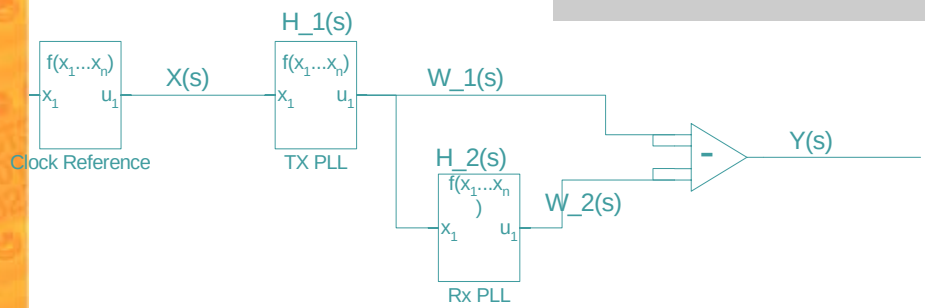
$$Y = X\,[1 - \exp(\ s * t\_delay\ )]$$

WAVECREST
Be certain of the signal you send.

PLL Based Transfer Function

- PLL Based DRC does not have delay dependencies
- PLL locks to the data rate and wants a high Rx PLL response for best performance



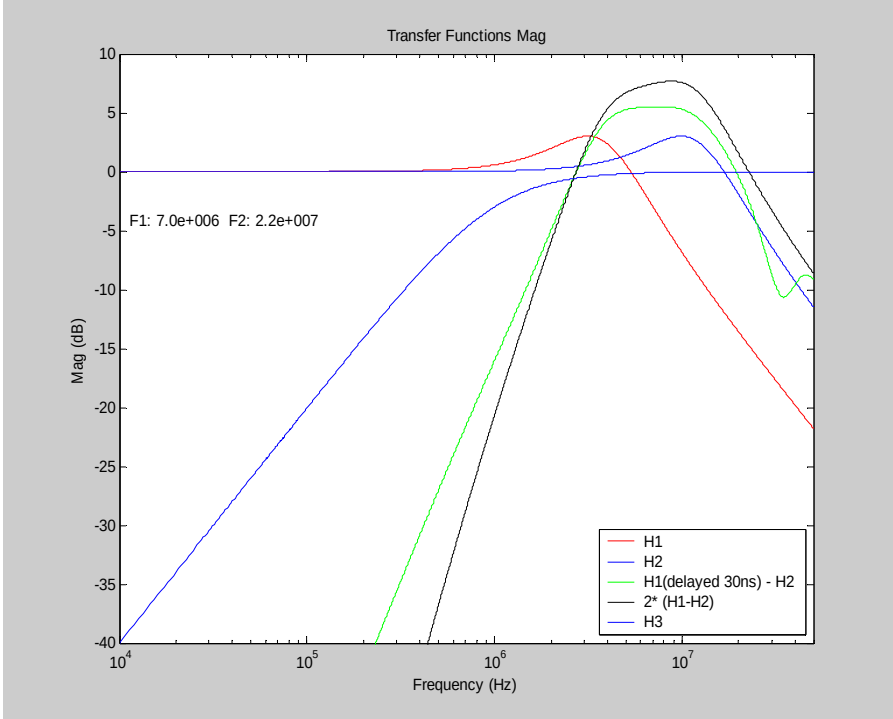


$$H_t(s) = H_1(s)\left(1 - H_2(s)\right)$$

WAVECREST
Be certain of the signal you send.

Digital PI Based Transfer Function

- The difference function includes an arbitrary phase delay not to exceed 30 ns
  - The delay “un-correlates” the clock/data and closes the eye
- This can be estimated with 2X multiplier of H1(s)-H2(s)



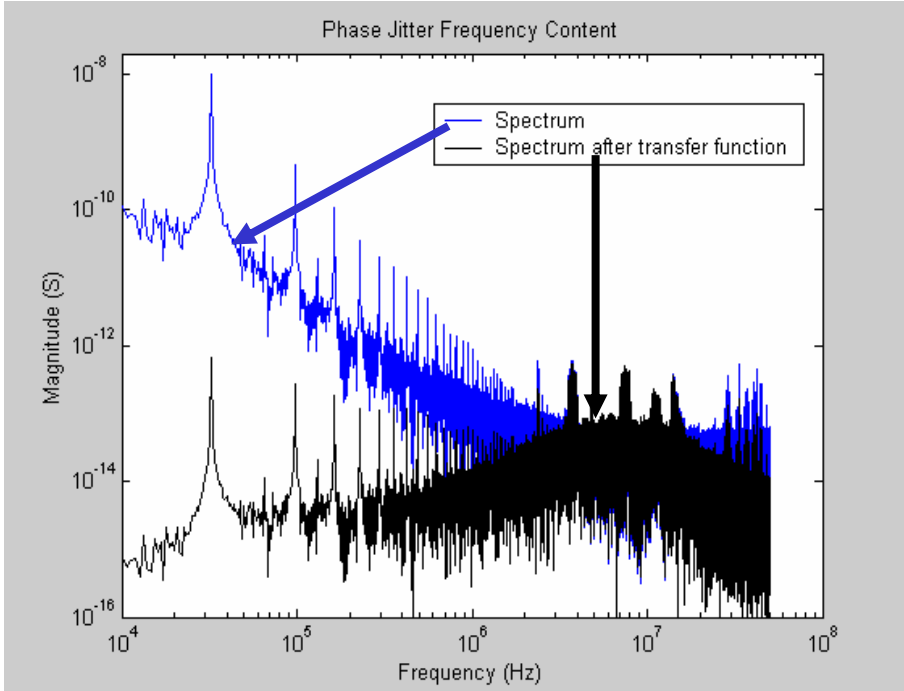
$$H_t(s) = 2\,[H_1(s) - H_2(s)]\,H_3(s)$$

WAVECREST
Be certain of the signal you send.

Models Applied to Measured Data

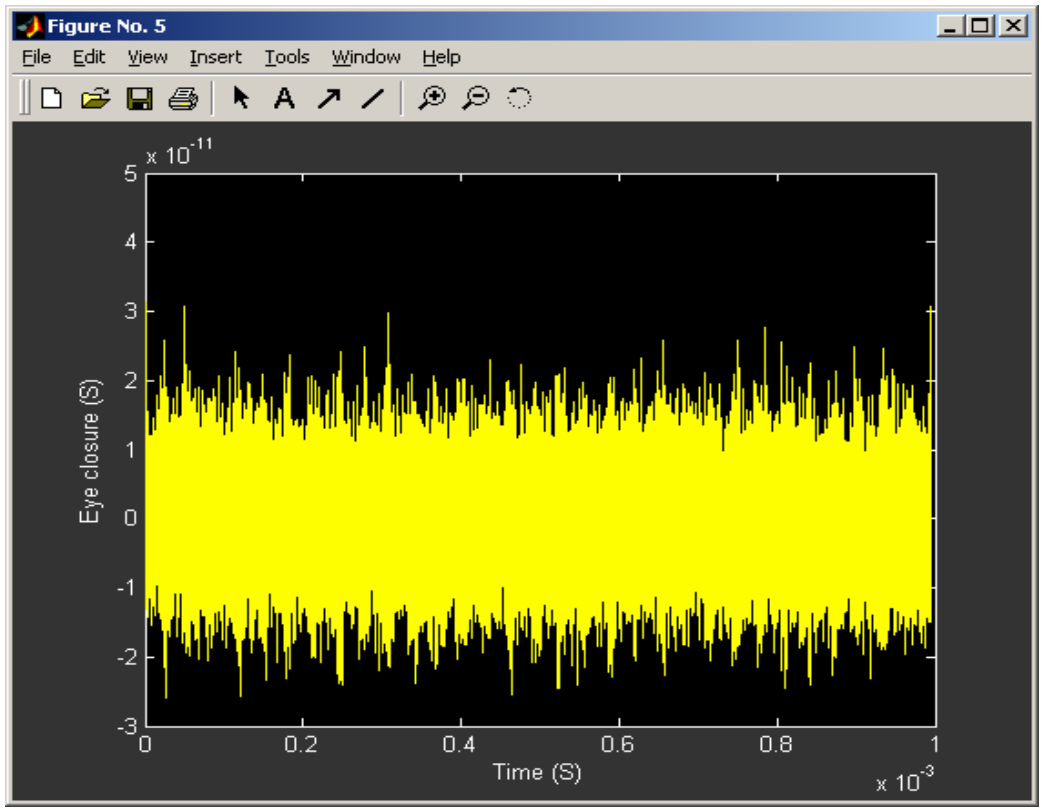
- X(s)
  - The input spectrum can be measured by measuring a clock and applying the jitter definitions to get the Phase Jitter
  - The Phase Jitter signal is then transformed into the Phase Jitter spectrum, X(s)
- H(s)
  - The models presented here give Ht(s), the bounding function, including the delay
- Y(s)

  Y(s) =X(s)H(s)



Eye-Closure at the Rx Sample Flop:One Method

- The inverse Laplace transform of Y(s) gives the eye closure in the time domain, y(t)



3.2 Link Jitter Budget

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Specified Overall System Jitter Budget (PCIe I)

Total System Jitter Budget

Jitter Contribution	Min Rj (ps) one sigma	Max Dj (ps) P-P	Tj at BER 10^{-12} (ps)	Tj at BER 10^{-6} (ps)
Tx	2.8	60.6	100	87
Ref Clock	4.7	41.9	108	86
Media	0	90	90	90
Rx	2.8	120.6	160	147
Linear Total Tj:			458	410
Root Sum Square (RSS) Total Tj:			399.13	371.52

IV: Generic Jitter, Noise, and BER (JNB) Test Requirements and Methods

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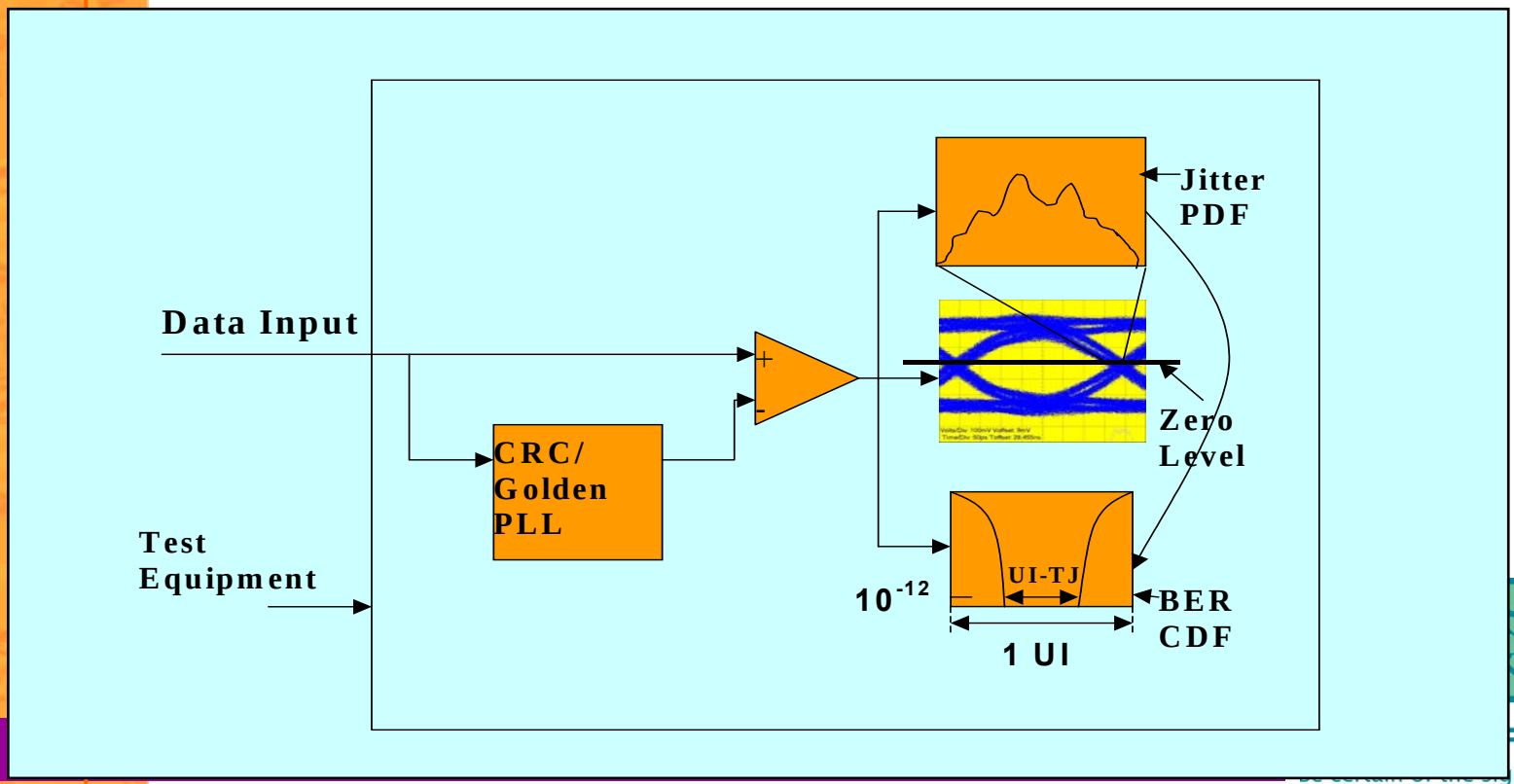
Be certain of the signal you send.

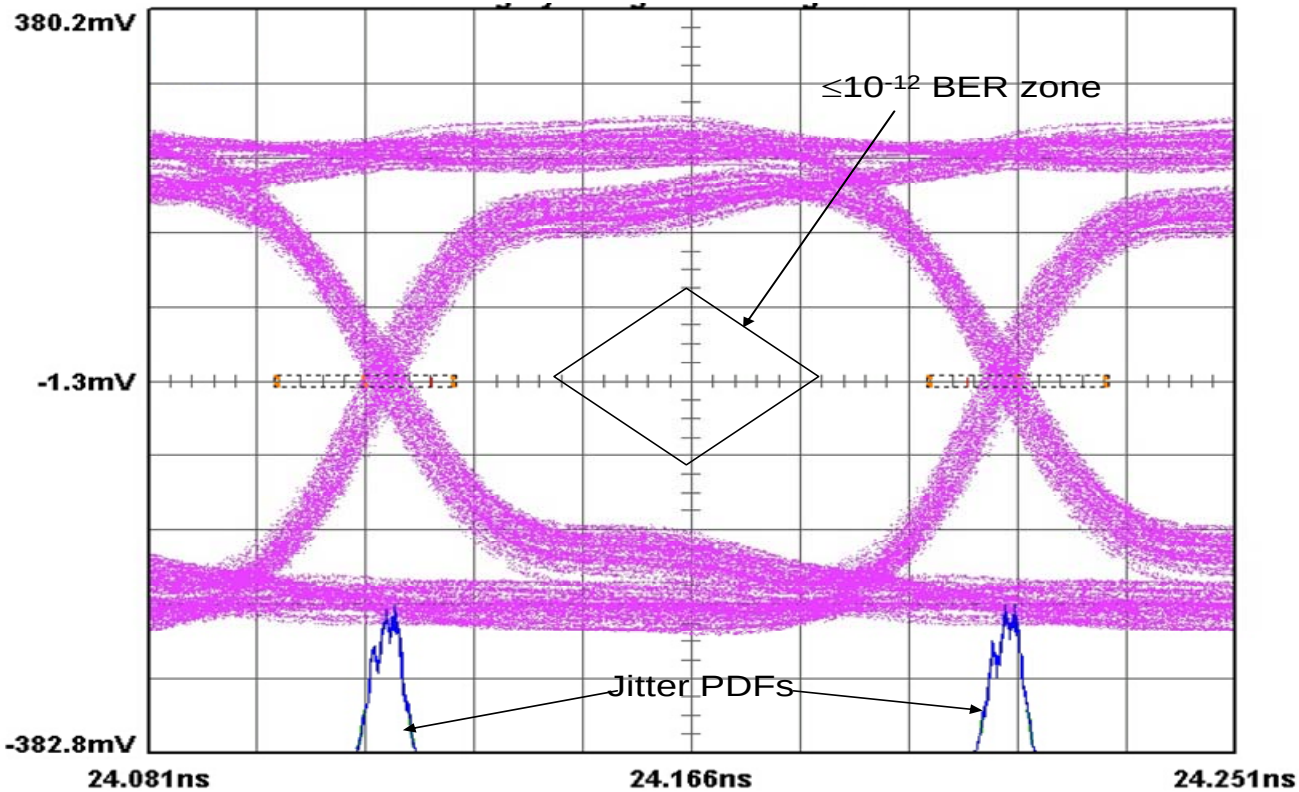
JNB Output Estimation/Measurement Requirements

- Measure clock-to-data jitter
- Measure DJ and RJ
- TJ is measured at BER = 10^{-12}



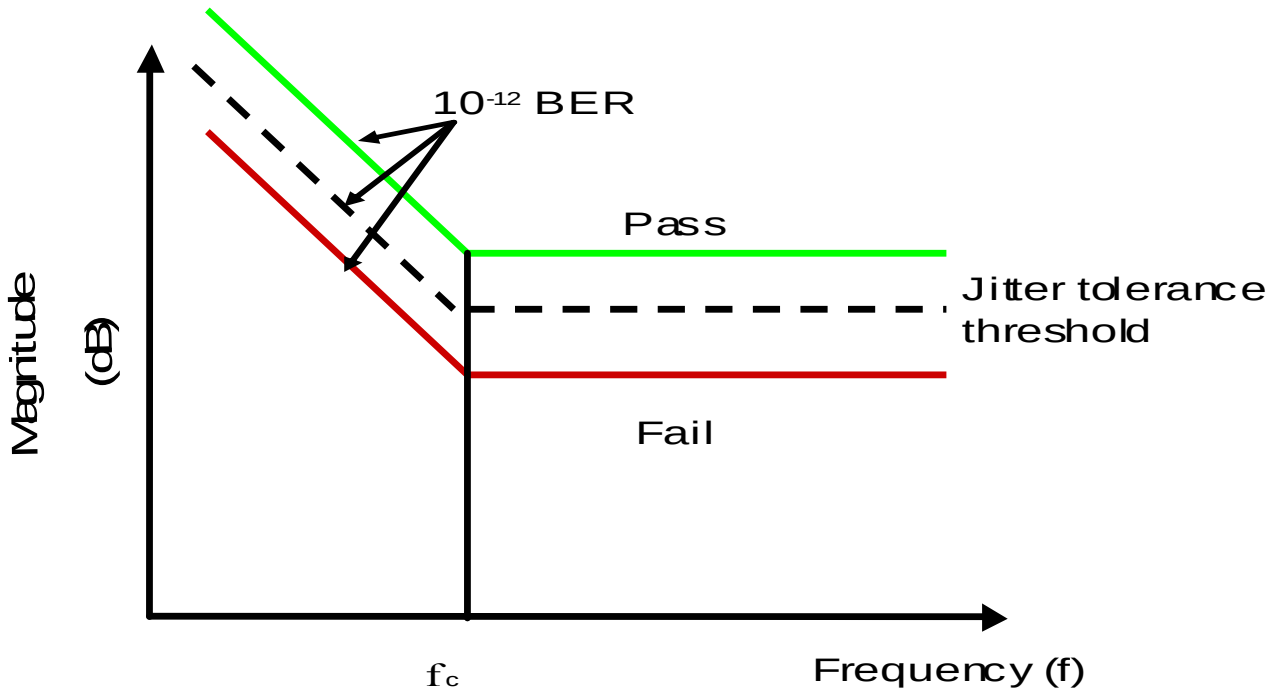
JNB Output Measurement Method

- CDR as the reference for eye-diagram measurement
- BER = 10^{-12} eye mask
- DJ, RJ, TJ, and DN, RN, TN estimation based on PDFs



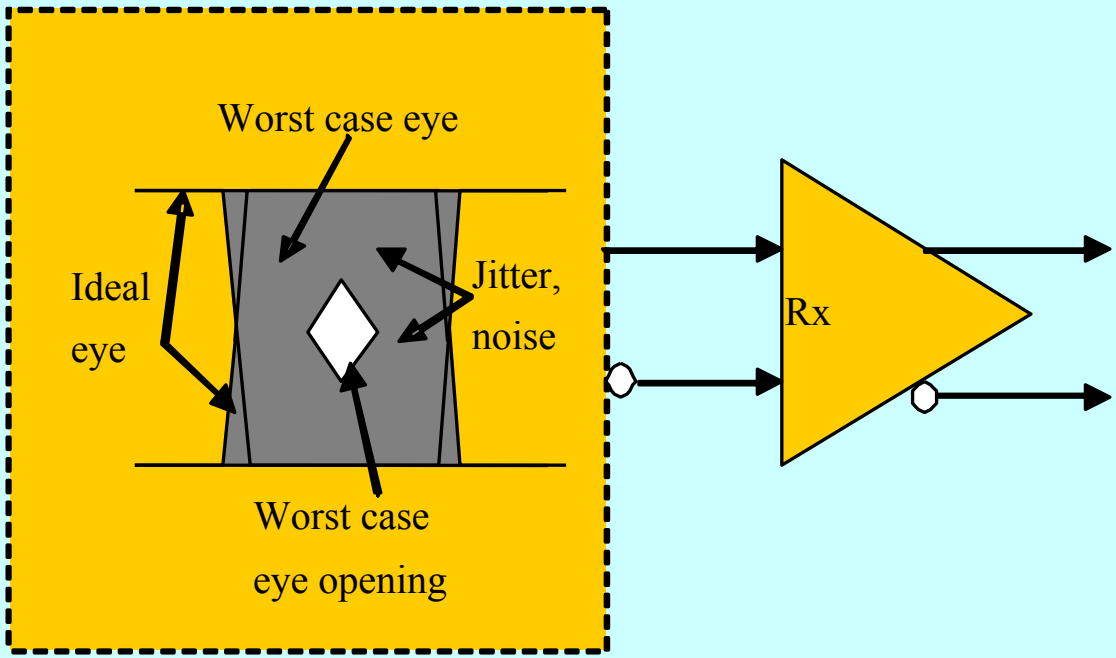
JNB Tolerance Test Requirements (I)

- Tolerance frequency response mask

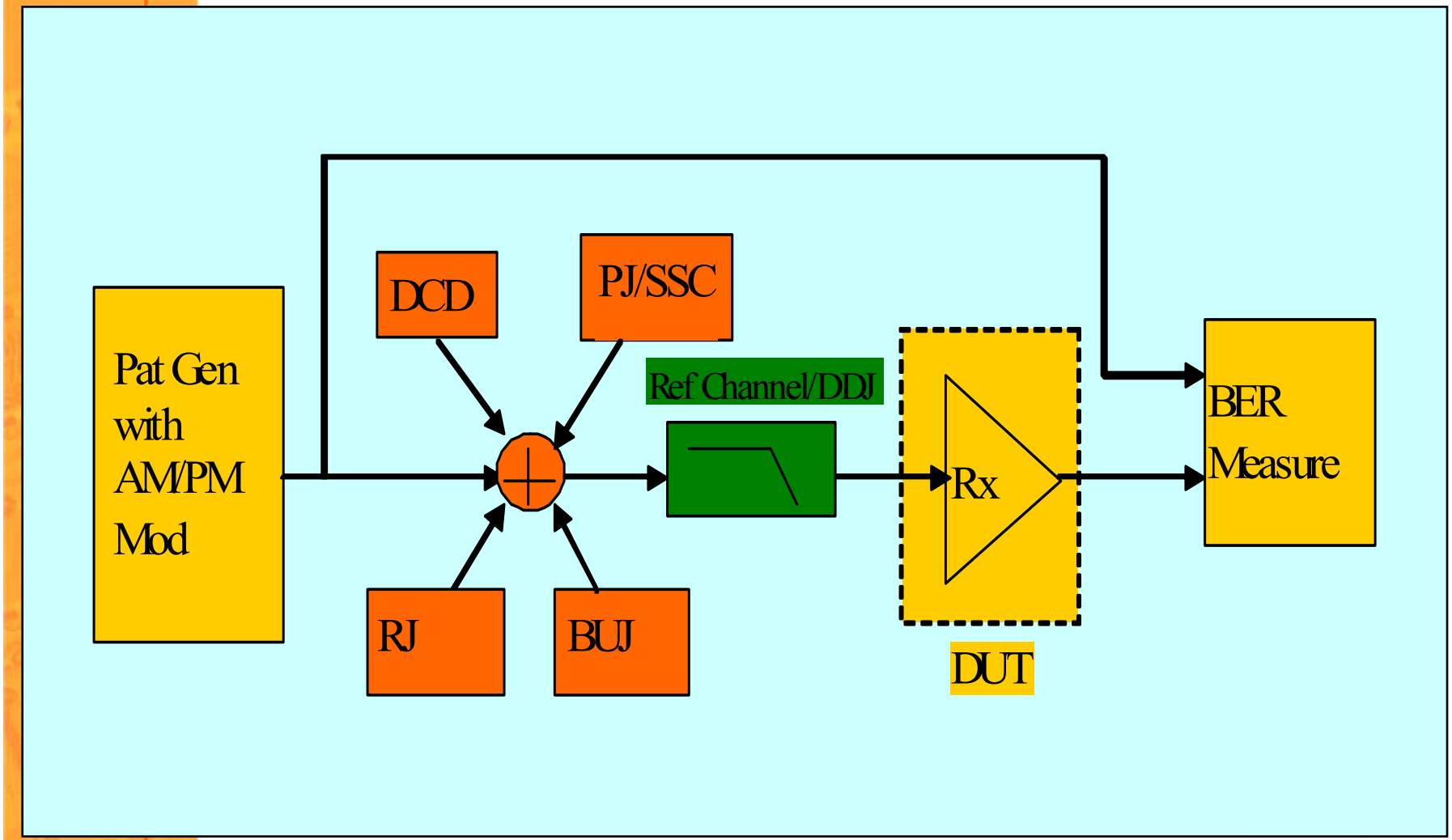


JNB Tolerance Test Requirements (II)

- Worst case eye mask attributing jitter and noise stressing



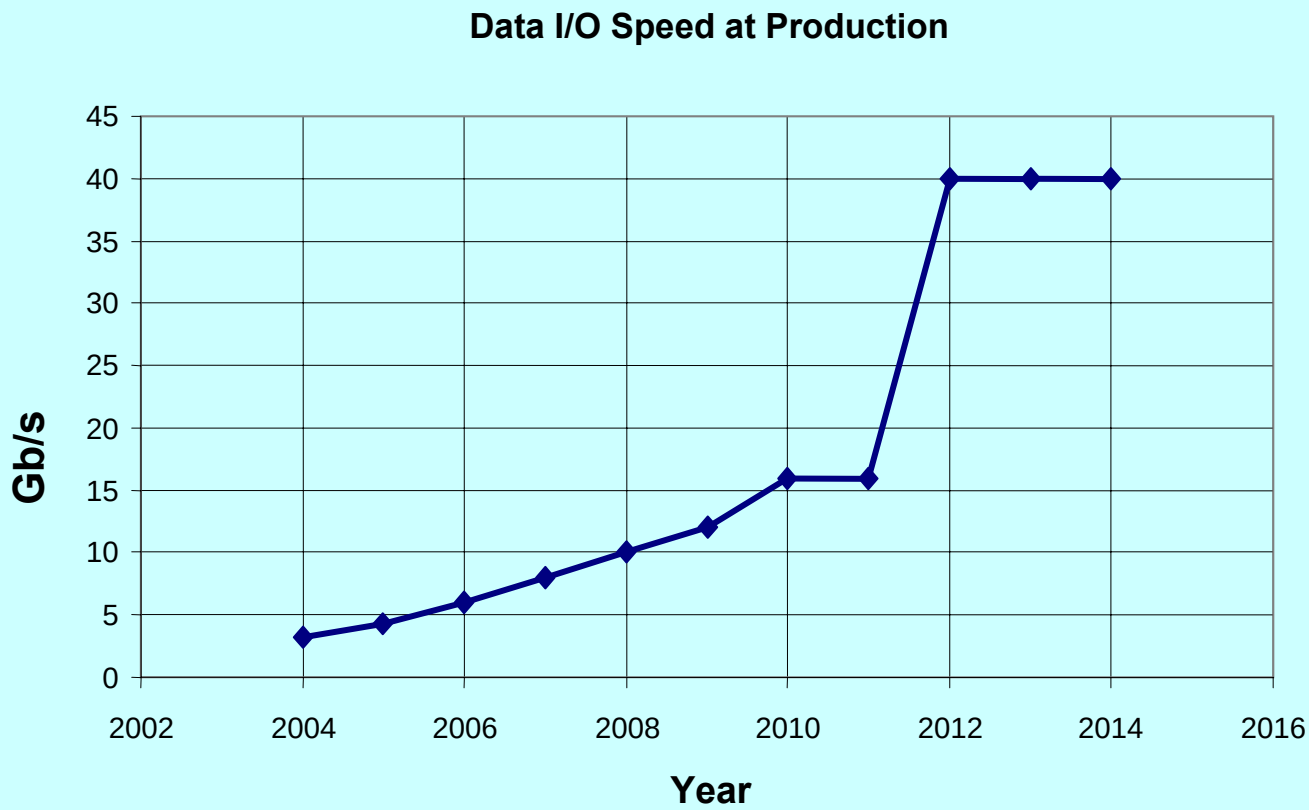
A Generic JNB Tolerance Test Method



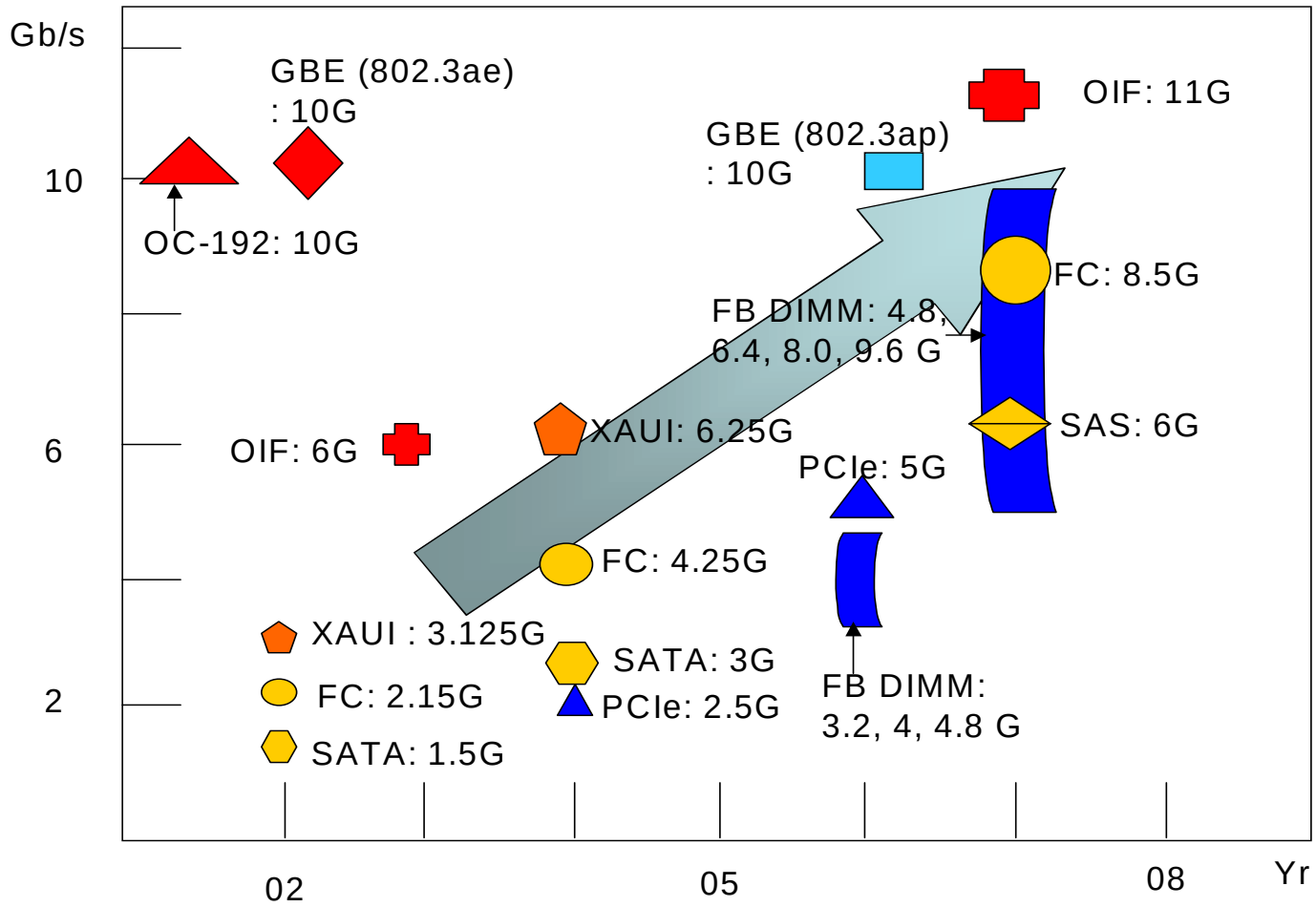
V: Jitter and Signaling Test in Gbps Link Standards

WAVECREST
Be certain of the signal you send.

ITRS High-Speed I/O Speed Roadmap



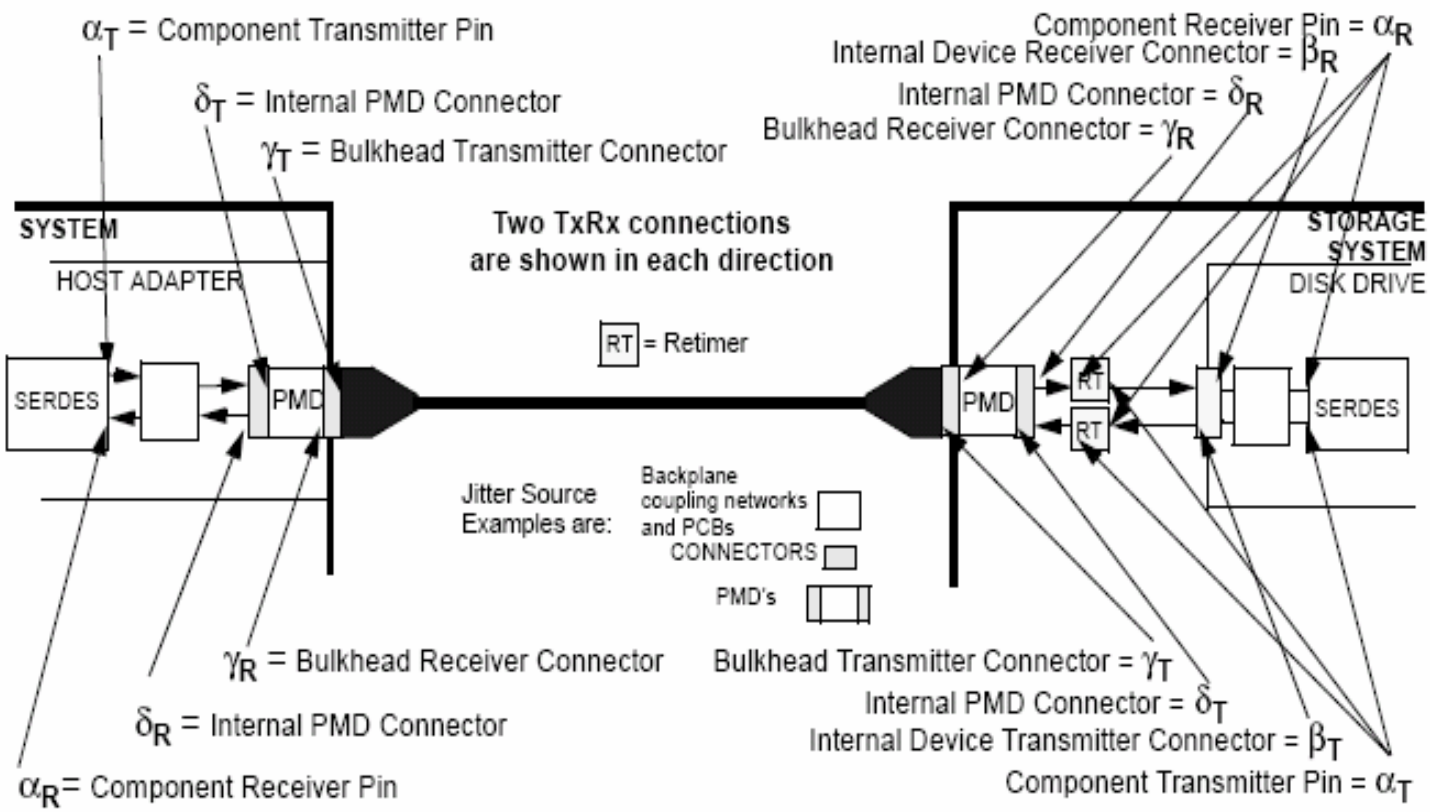
Multiple Gb/s Link Standard Technology Roadmaps



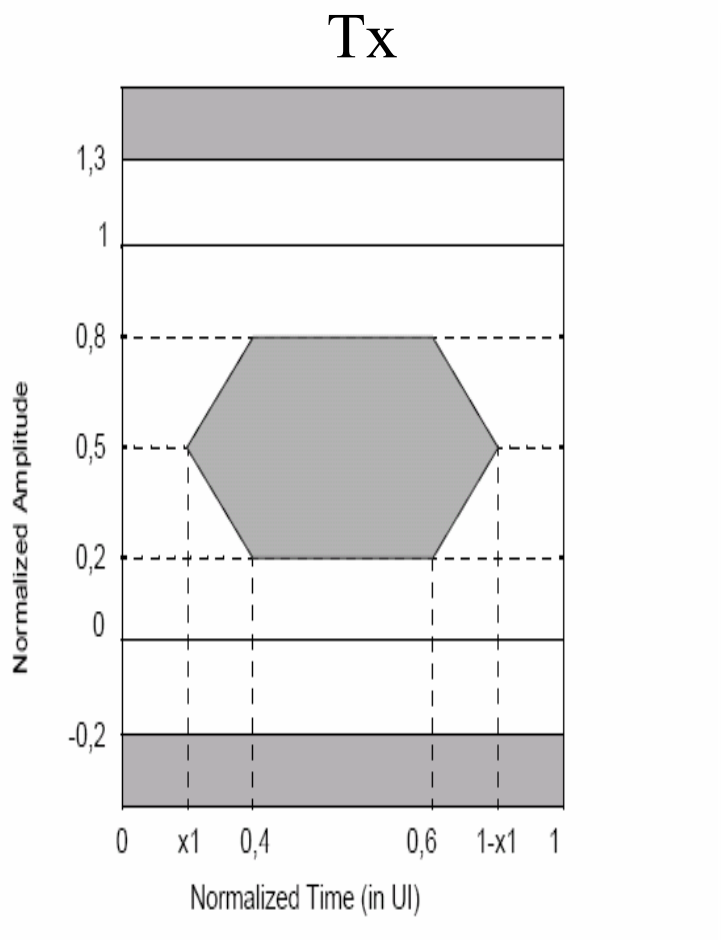
5.1 Fibre Channel (FC) JNB and Signaling Test Overview

WAVECREST
Be certain of the signal you send.

FC Testing Point Definition



FC Compliance Eye-Masks



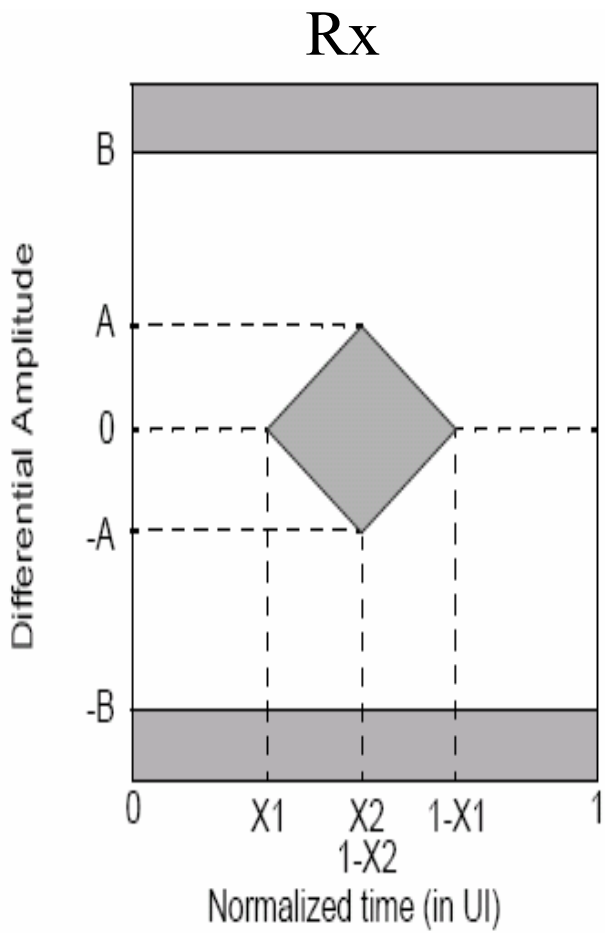


Figure 38 – Eye diagram mask at β_R, δ_R, and γ_R

Jitter Output Requirements

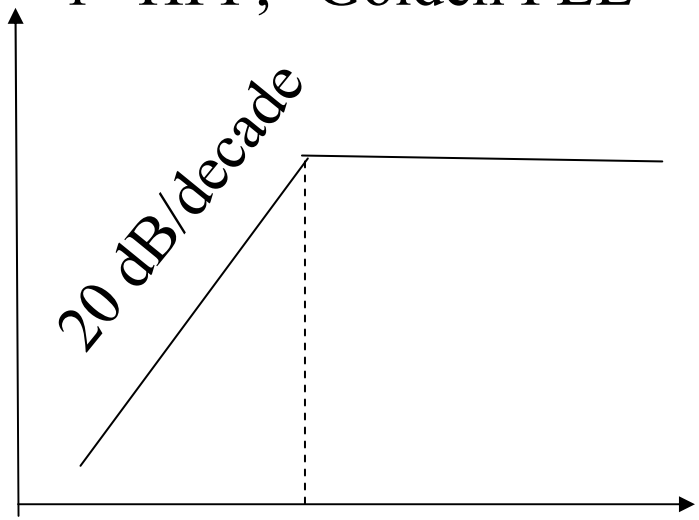
Table 9 – SM jitter output, pk-pk, max

100-SM-LC-L									
	Unit	α_T	β_T	δ_T	γ_T	γ_R	δ_R	β_R	α_R
Deterministic (DJ)[3]	UI	note 4	0,11	0,12	0,21	0,23	0,36	0,37	note 4
Total (TJ)[1,2,3]	UI	note 4	0,23	0,25	0,43	0,47	0,61	0,63	note 4
200-SM-LC-L									
	Unit	α_T		δ_T	γ_T	γ_R	δ_R		α_R
Deterministic (DJ)[3]	UI	note 4		0,14	0,26	0,28	0,39		note 4
Total (TJ)[1,2,3]	UI	note 4		0,26	0,44	0,48	0,64		note 4
400-SM-LC-L									
	Unit	α_T		δ_T	γ_T	γ_R	δ_R		α_R
Deterministic (DJ)[3]	UI	note 4		0,14	0,26	0,28	0,39		note 4
Total (TJ)[1,2,3]	UI	note 4		0,26	0,44	0,48	0,64		note 4

Notes:
1 Total jitter is the sum of deterministic jitter and random jitter. If the actual deterministic jitter is less than the maximum specified, then the random jitter may increase as long as the total jitter does not exceed the specified maximum total jitter.
2 Total jitter is specified at the 10^{-12} probability.
3 The signal shall be measured using a jitter timing reference, e.g. Golden PLL, that approximates a single pole (20dB / decade) low pass filter with {corner frequency of the signaling rate / 1667}.
4 Values at the α points are determined by the application.

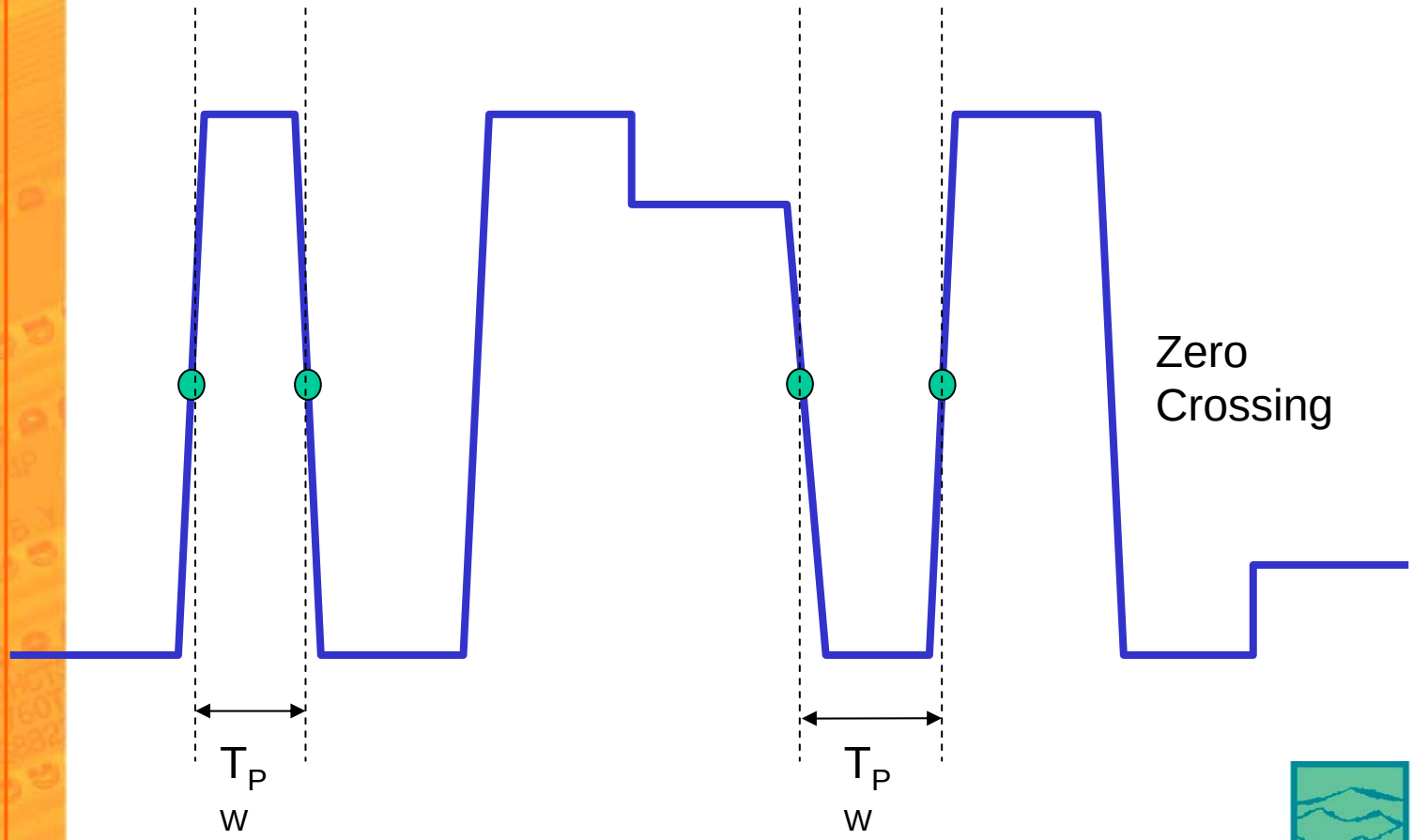
Jitter Transfer Function:

1st HPF, "Golden PLL"



$Fc = f_{BR}/1667$

New Test Parameter in FC 8X: (Pulse Width Shrinkage(PSW)



SAS JNB and Signaling Test

- SAS JNB and signaling test specifications are largely adopted from FC. Most of the testing requirements and methods for FC introduced will apply to SAS.

5.2 PCIe JNB and Signaling Test Overview

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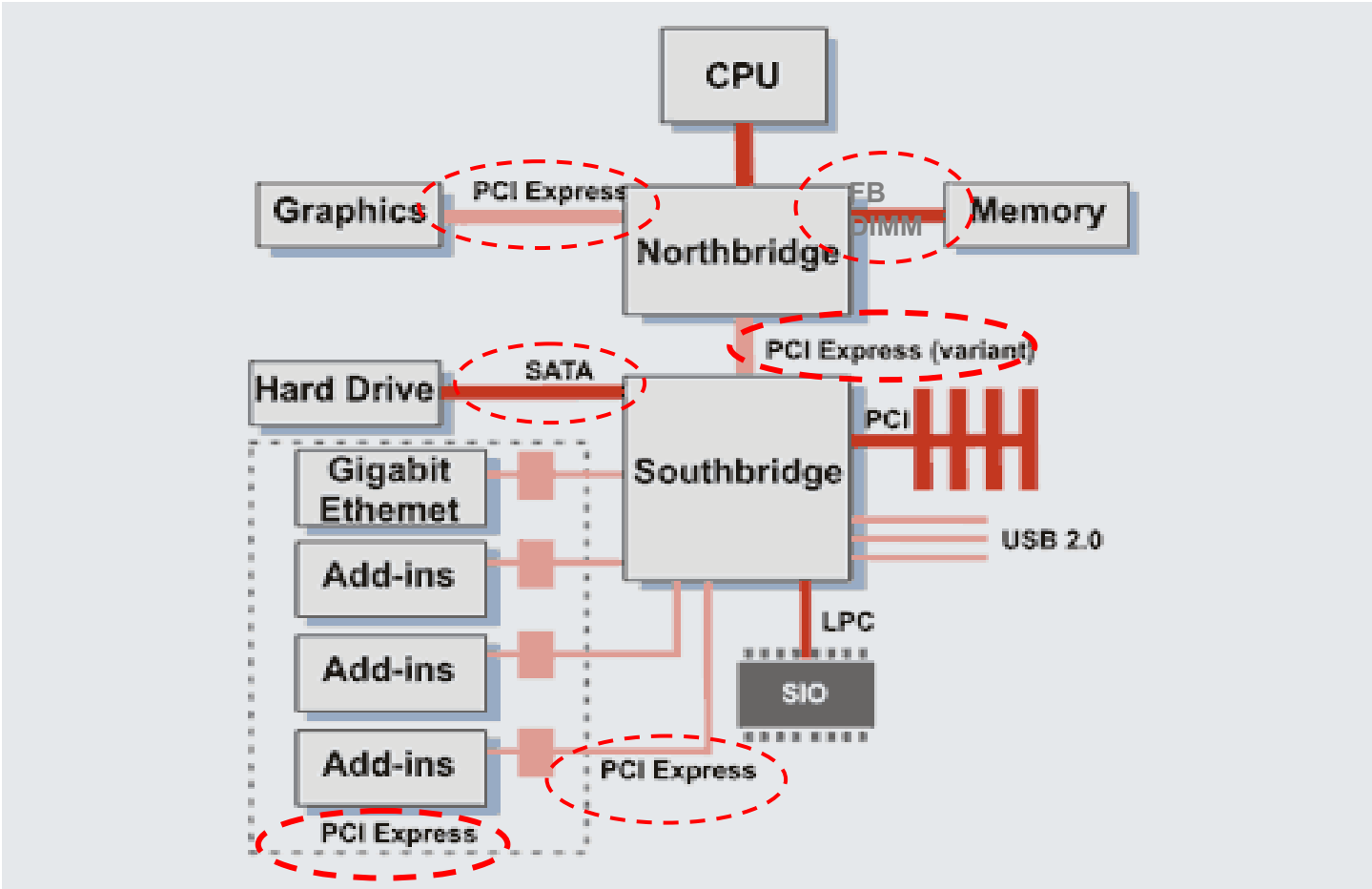
Be certain of the signal you send.

PCI Express Applications



Highlights of Changes Reference Clock Specification in PCIe

- The CEM specification is responsible for defining and specifying the 100 MHz reference clock on the connector. The current specification specifies voltage levels and ***Cycle-to-Cycle Jitter***. This has been shown[2] to be ***insufficient*** to fully bound the system, and a Phase Jitter specification is required. The change is to add a specification bounding the peak-peak magnitude reference clock jitter in the Phase Jitter domain.

- This change is meant to constrain the REFCLK Phase Jitter frequency spectrum for various Tx-Rx combinations by specifying the maximum amount of REFCLK Phase Jitter under a fixed filter characteristic.

- The PCI Express base specification provides the budget for TJ at a bit error rate (BER) of 10^{-12}. This *does not make any assumption or quantification* of Random Jitter. This change includes a minimum assumption for a system budget of Random Jitter and re-calculates the eye openings appropriately for a measurement specification at a BER of 10^{-6}.

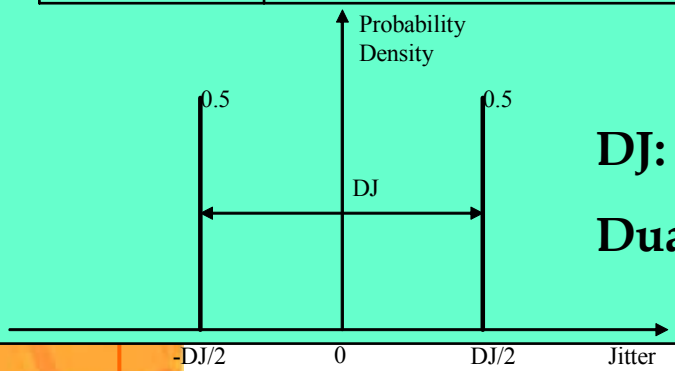
WAVECREST
Be certain of the signal you send.

Tx Amplitude Voltage Test Requirements

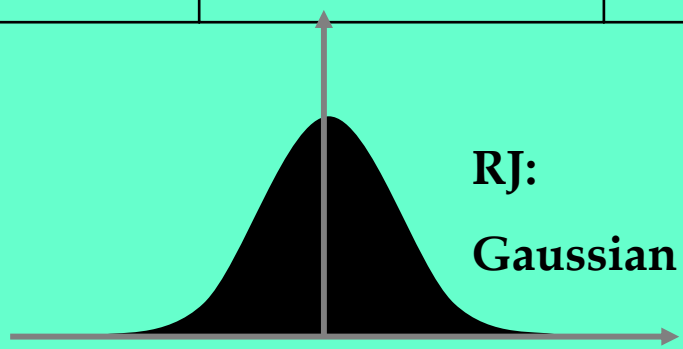
Symbol	Parameter and Definition	Gen I (2.5 Gb/s)	Gen II (5 Gb/s)	Unit
VTX-DIFF-PP	Differential p-p Tx voltage swing	0.8 (min) 1.2 (max)	**0.8 (min)** **1.2 (max)**	V
VTX-DE-RATIO -	Tx de-emphasis level	3.0 (min) -4.0 (max)	**-5.5 (min)** **-6.5 (max)**	dB

Tx Jitter/Timing Test Requirements

Symbol	Parameter and Definition	Gen I (2.5 Gb/s)	Gen II (5 Gb/s)	Unit
TMIN-PULSE	Instantaneous pulse width	Not spec'ed	**0.9 (min)**	UI
TTX-EYE	Transmitter Eye opening (@10^{-12} BER) including all jitter sources	0.75 (min)	**0.75 (min)**	UI
TTX-DJ-DD (max)	Tx deterministic jitter (DJ)	Not spec'ed	**0.15 (max)**	UI



DJ: Dual-Dirac



RJ: Gaussian

Tx PLL Test Requirements

Symbol	Parameter and Definition	Gen I (2.5 Gb/s)	Gen II (5 Gb/s)	Unit
BWTX-PLL	Maximum Tx PLL Bandwidth (BW)	22 (max)	**16 (max)**	MHz
BWTX-PLL-LO-3DB	Minimum Tx PLL BW for 3 dB peaking	3 (min)	**8 (min) MHz**	MHz
BWTX-PLL-LO-1DB	Minimum Tx PLL BW for 1 dB peaking	Not spec'ed	**5 (min)**	MHz
PKGTX-PLL1	Tx PLL peaking with 8 MHz min BW	Not spec'ed	**3.0 (max)**	dB
PKGTX-PLL2	Tx PLL peaking with 5 MHz min BW	Not spec'ed	**1.0 (max)**	dB

Tx Test Jitter Transfer Function

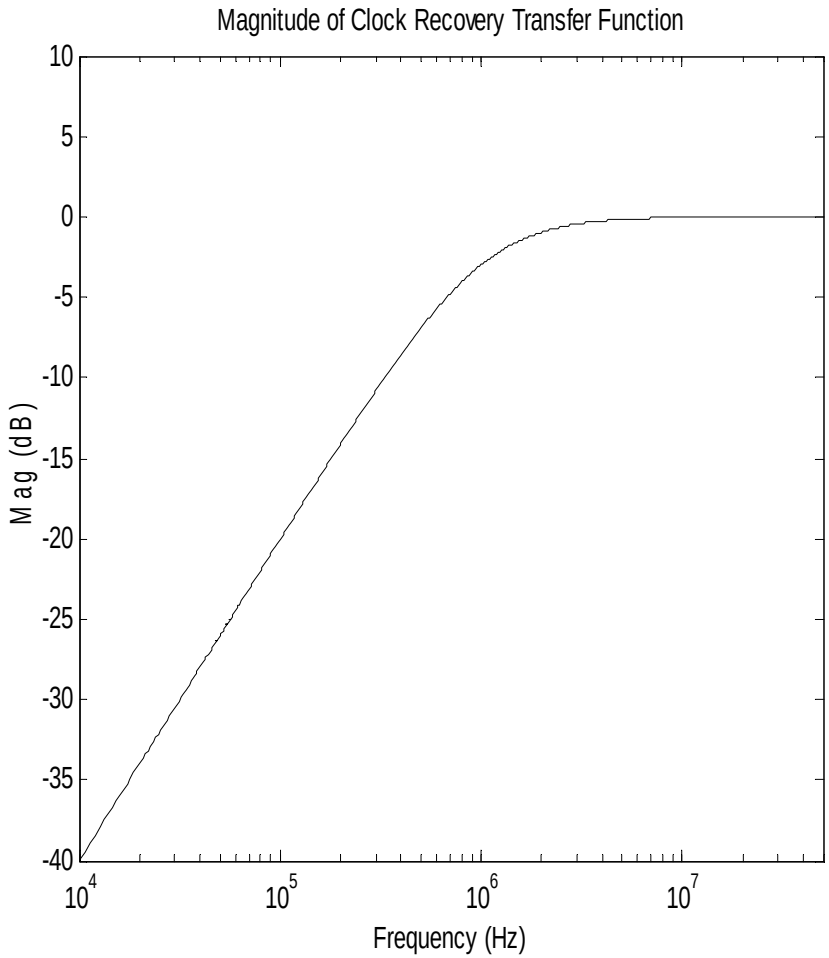
- 1st -order HPF of

$$H_3(s) = \frac{s}{s + \omega_3}$$

where

$$\omega_3 = 2\pi f_3$$

$$f_3 = 1.0\,MHz$$



Reference Clock Test Requirements

Symbol	Parameter and Definition	Min	Max	Unit
TPERIOD-ABS	Averaged instantaneous period (including SSC)	9.997	10.053	ns
VIH VIL	Differential Input High Voltage Differential Input Low Voltage	+150	-150	mV
VRB	Ring-back Voltage Margin	-100	+100	mV
$(dV/dt)_R$	Rising Edge Rate	0.6	4.0	V/ns
$(dV/dt)_F$	Falling Edge Rate	0.6	4.0	V/ns
η_{DC}	Duty Cycle	40	60	%
TCLK_RJ	**Ref clk RMS jitter**		**3.1**	**ps**
TSSC-JITTER-CC	SSC induced jitter that a receiver must track. Relevant only for common clock architecture		65 ps PP at 33 KHz	ps
TSSC-JITTER-DDC	SSC induced jitter that a receiver must track. Relevant only for data driving PLL architecture		20 ns PP at 33 KHz	ns

Reference Clock Jitter Transfer Function

$$H(s) = \left[H_1(s) * e^{-s * t\_delay} - H_2(s) \right]$$

$$H_1(s) = \frac{2s\zeta\omega_1 + \omega_1^{\,2}}{s^2 + 2s\zeta\omega_1 + \omega_1^{\,2}}$$

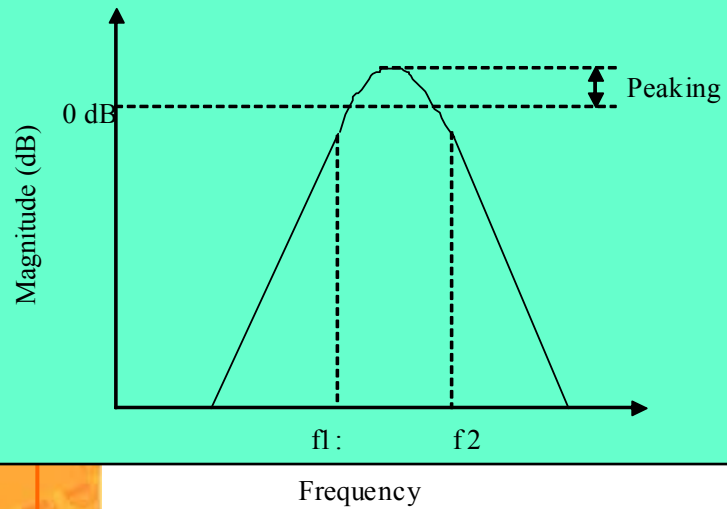
$$H_2(s) = \frac{2s\zeta\omega_2 + \omega_2^{\,2}}{s^2 + 2s\zeta\omega_2 + \omega_2^{\,2}}$$

$$\zeta = 0.54$$

$$\omega_1 = \frac{2 * \pi * 8.61 * 10^6}{\sqrt{1 + 2\zeta^2 + \sqrt{\left(1 + 2\zeta^2\right)^2 + 1}}} Rad/s$$

$$\omega_2 = \frac{2 * \pi * 4.31 * 10^6}{\sqrt{1 + 2\zeta^2 + \sqrt{\left(1 + 2\zeta^2\right)^2 + 1}}} Rad/s$$

$$t\_delay = 12 \cdot 10^{-9}\, s$$



Rx Amplitude Voltage Test Requirements

Symbol	Parameter and Definition	Gen I (2.5 Gb/s)	Gen II (5 Gb/s)	Unit
VRX-DIFF-PP	Differential p-p Rx voltage swing	0.175 (min) 1.2 (max	**0.120 (min)** **1.2 (max)**	V
VRX-MAX-MIN-RATIO	Max to Min pulse voltage on consecutive UI	Not spec'ed	**5 (max)**	

Rx Jitter/Timing Test Requirements

Symbol	Parameter and Definition	Gen I (2.5 Gb/s)	Gen II (5 Gb/s)	Unit
TRX-EYE	Receiver Eye opening (@10^{-12} BER)	0.4 (min)	**0.4 (min)**	UI
TRX-DJ-DD (max)	Rx deterministic jitter (DJ)	Not spec'ed	**0.44 (max)**	UI

5.3 FB DIMM JNB and Signaling Test Overview

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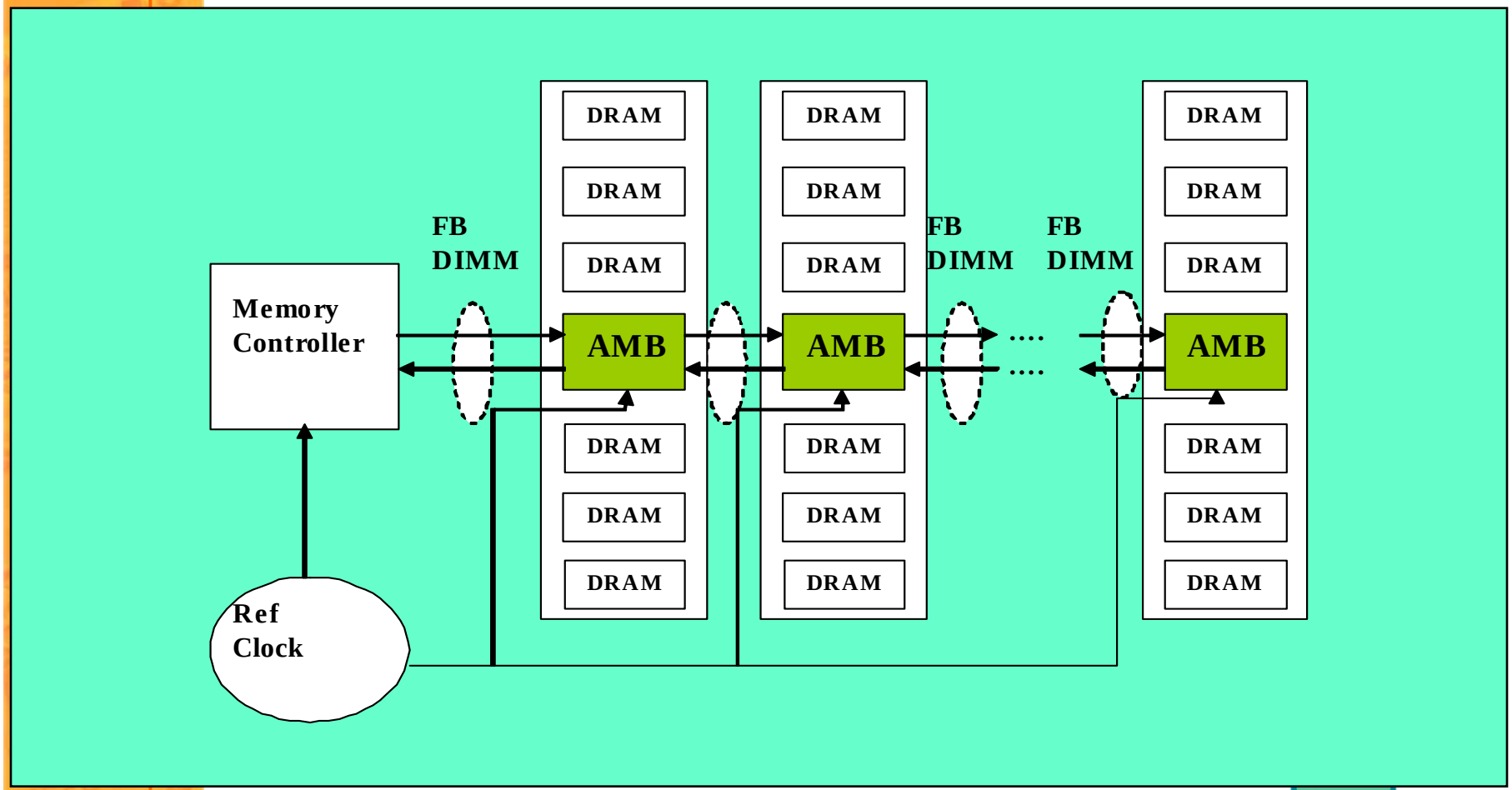
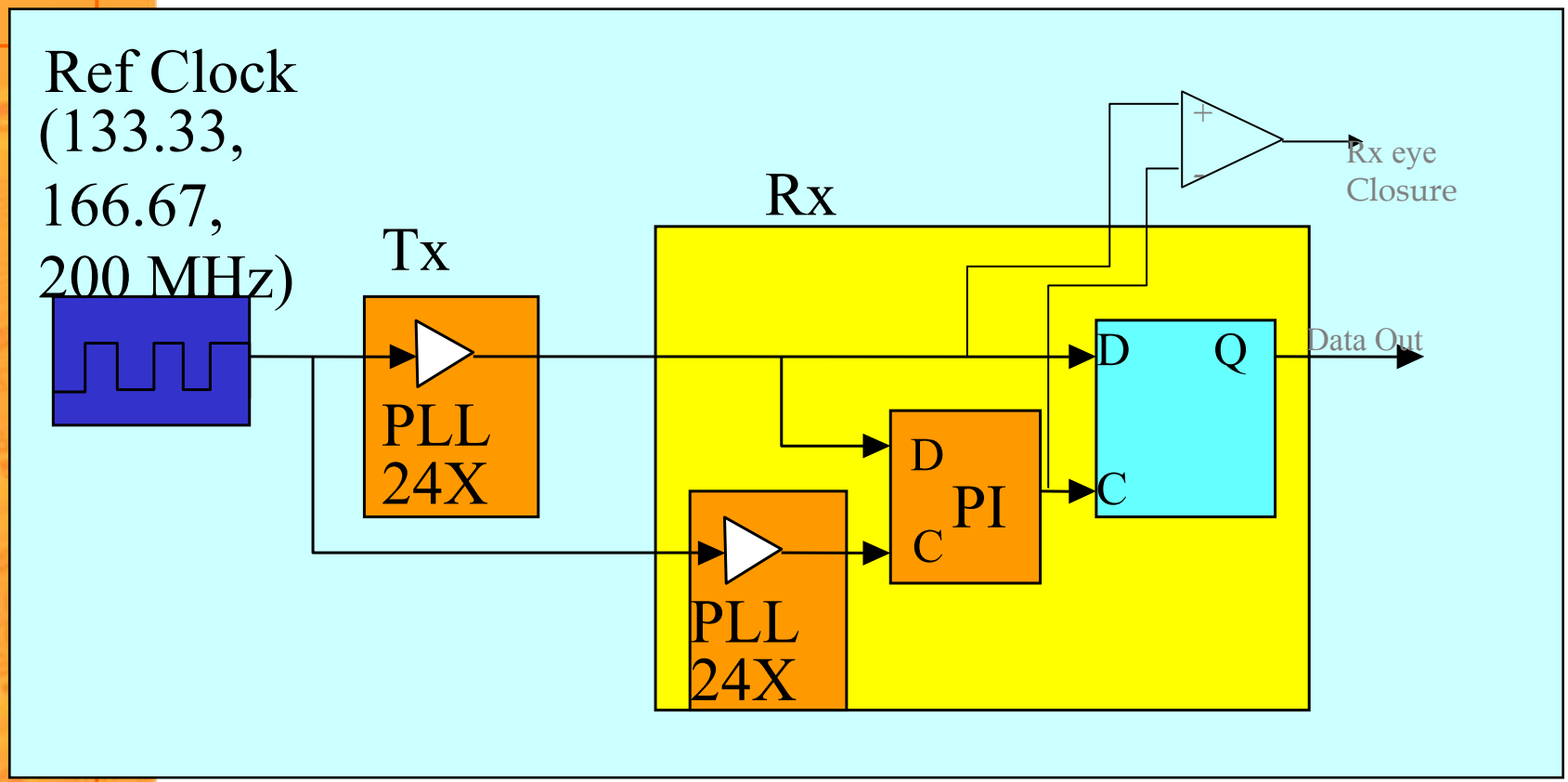
Be certain of the signal you send.

FB DIMM Applications



FB DIMM Link Architecture



- Very similar to PCIe
- Resulting in similar test requirements

Other High-Speed I/O Link Tests

- FB DIMM link architectures are not much different from that of PCI Express

- Test Methods illustrated can apply well for those and similar link standards

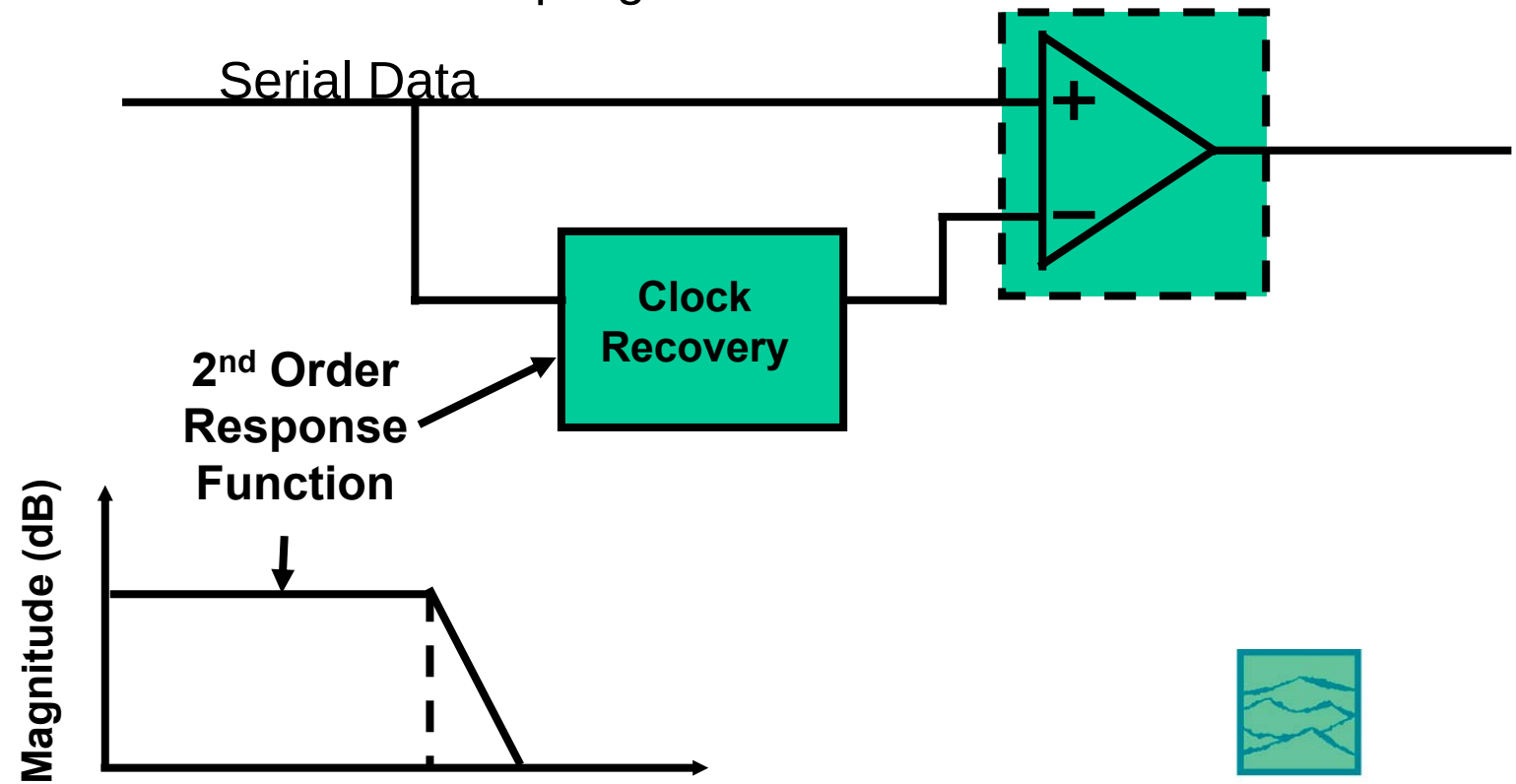
5.4 SATA JNB and Signaling Test Overview

WAVECREST
Be certain of the signal you send.

Data Recovery Circuits (DRC)

- SATA DRC are implemented by two types of clock recovery:

  PLL or over-sampling



SATA II 1.0 DCR Jitter Transfer Function

- S-domain jitter transfer function H(s) is:

$$H_{HP}(s) = 1 - \frac{2s\zeta\omega_1 + \omega_1^2}{s^2 + 2s\zeta\omega_1 + \omega_1^2}$$

Where

$$\zeta_{min} = 0.707 \;,\; \zeta_{max} = 1.00$$

$$\omega_1 = \frac{2\pi f_c}{\sqrt{1 + 2\zeta^2 + \sqrt{\left(1 + 2\zeta^2\right)^2 + 1}}} \; Rad \;/\; s$$

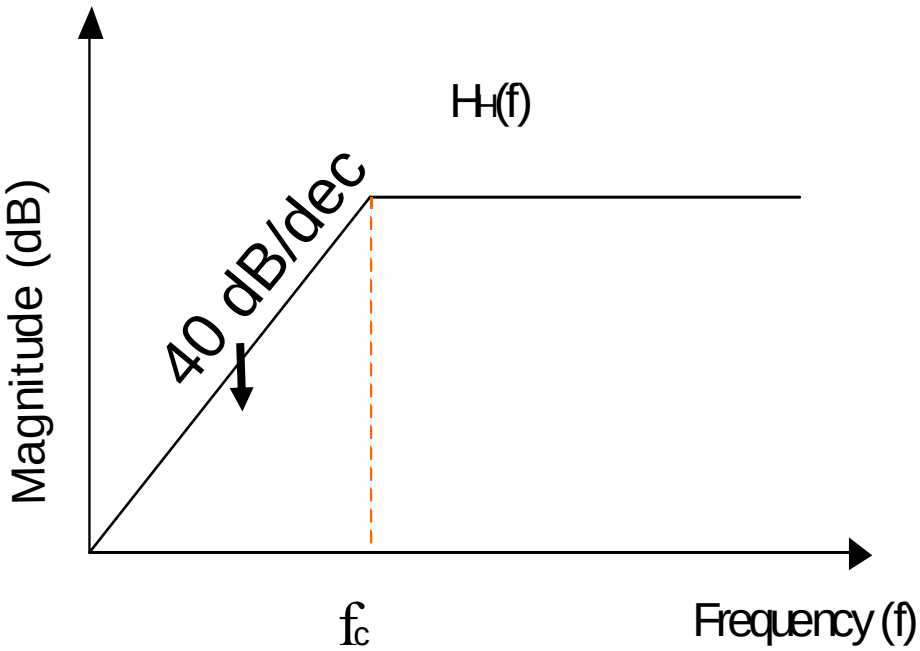
$$f_c = \frac{f_{BAUD}}{10}, \frac{f_{BAUD}}{500}, \frac{f_{BAUD}}{1667}$$

$$f_{BAUD} = 3.0 \times 10^9 \text{ Hz}$$

$$s = j\omega, \quad \text{and} \quad \omega = 2\pi f$$

WAVECREST
Be certain of the signal you send.

Jitter Transfer Function Graph



- A 2nd order high-pass function

5.5 JNB and Signaling Test Requirements Summary for Key Gbps Link Standards

WAVECREST
Be certain of the signal you send.

Network Centric Link Standards JNB and Signaling Test Requirements and Parameters

	SONET	GBE (802.3ae)	XAUI	GBE (802.3ap)	OIF
Tx:					
TJ, DJ, RJ	N	Y	Y	Y	Y
Band p-p &rms	Y	N	N	N	N
CR H(s)	Y	Y	Y	Y	Y
Eye mask	N	Y	Y	Y	Y
Rx:					
CR H(s) Stressing	Y	Y	Y	Y	Y
Jitter, DJ,RJ Stressing	N	Y	Y	Y	Y
Amplitude Eye Stressing	N	Y	Y	Y	Y
Others:					
Ref Clk	N	N	N	N	N
PLL	N	N	N	N	N
BER	10^{-12}	10^{-12}	10^{-12}	10^{-12}	10^{-15}

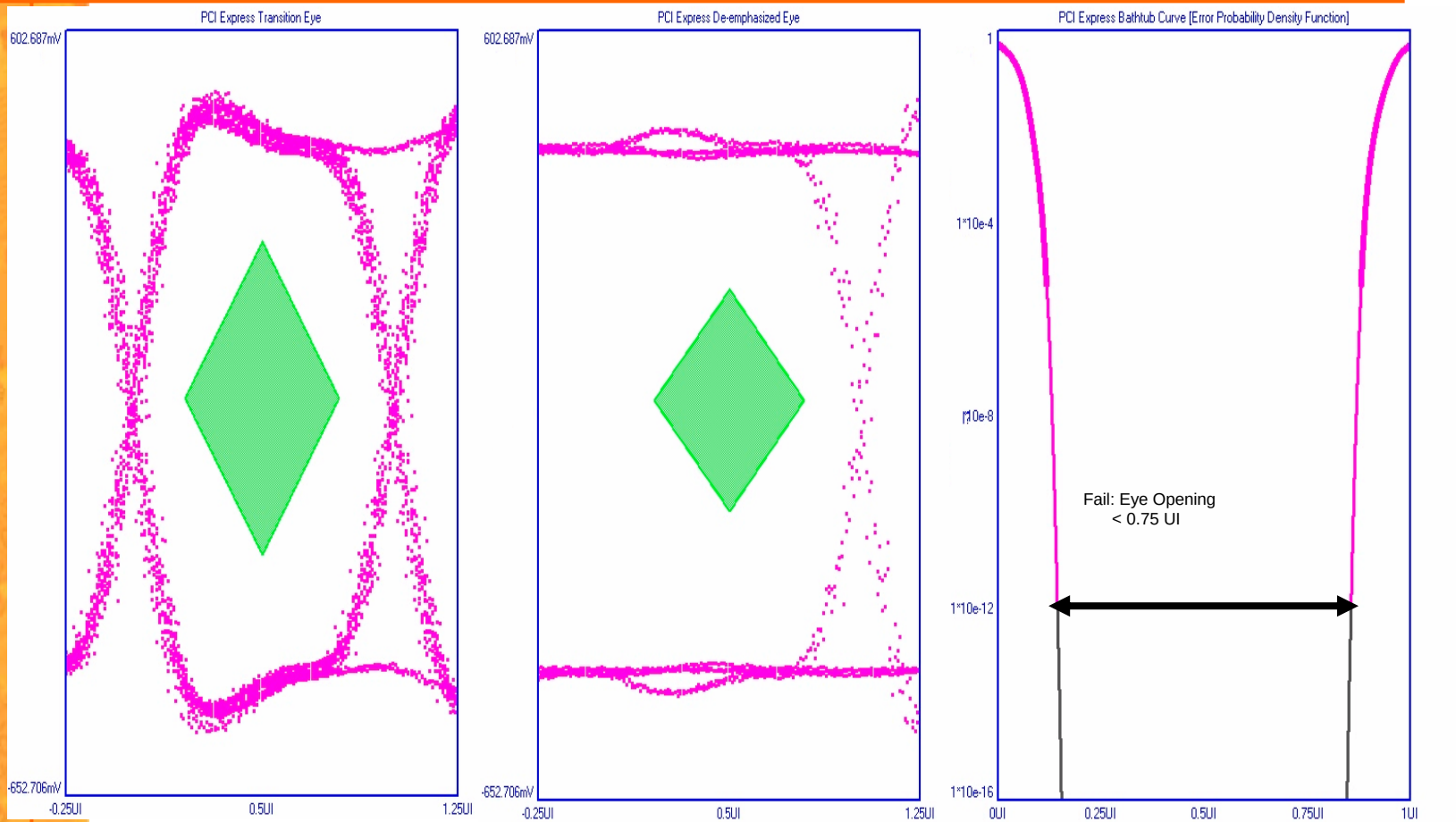
Computer Centric Link Standards JNB and Signaling Test Requirements and Parameters

	PCIe	FB DIMM	FC	SATA
Tx:				
TJ, DJ, RJ	Y	Y	Y	Y
Band p-p &rms	N	N	N	N
CR H(s)	Y	N	Y	Y
Eye mask	Y	Y	Y	Y
Rx:				
CR H(s) Stressing	Y	N	Y	Y
Jitter, DJ,RJ Stressing	Y	Y	Y	Y
Amplitude Eye Stressing	Y	Y	Y	Y
Others:				
Ref Clock	Y	Y	N	N
PLL	Y	Y	N	N
BER	10^{-12}	10^{-12}	10^{-12}	10^{-12}

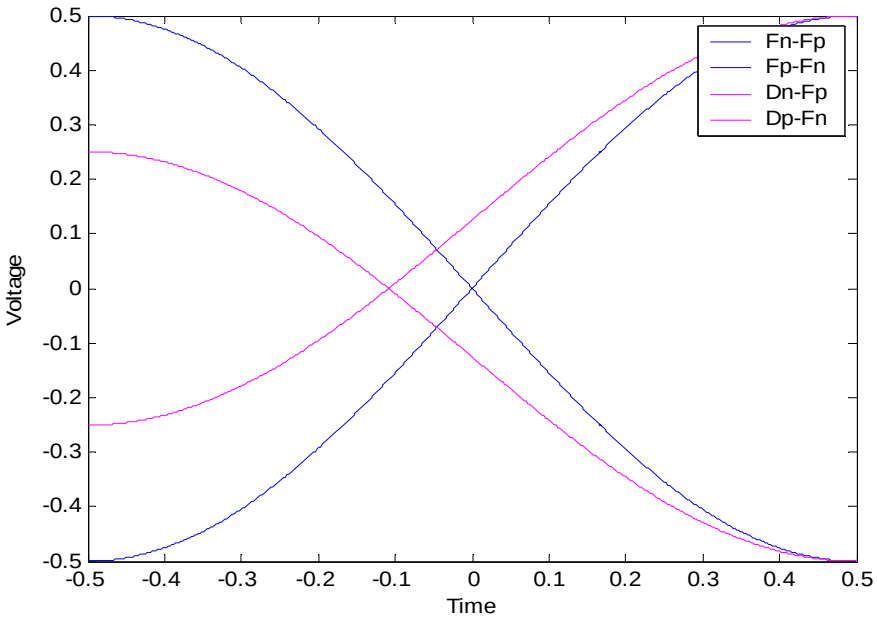
5.5 Application and Case Study Examples

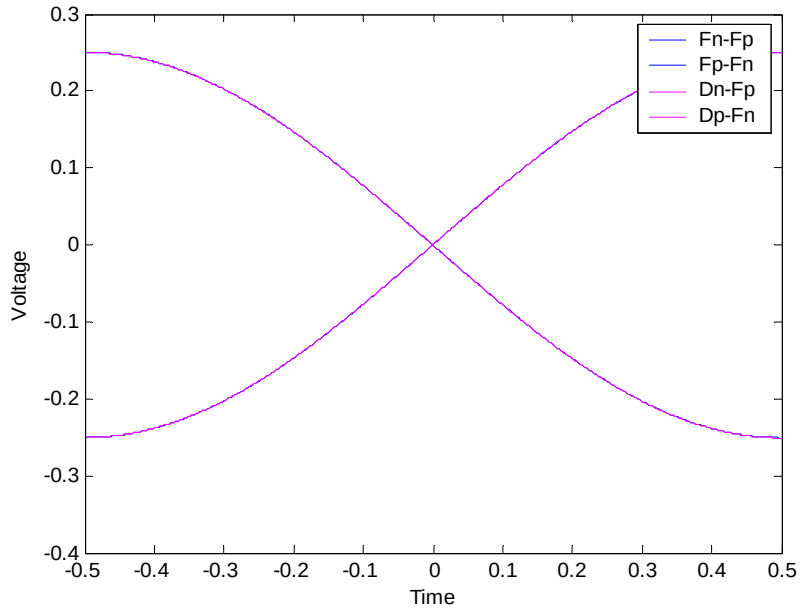
WAVECREST
Be certain of the signal you send.

Tx JNB Compliance Test Example (PCIe II)

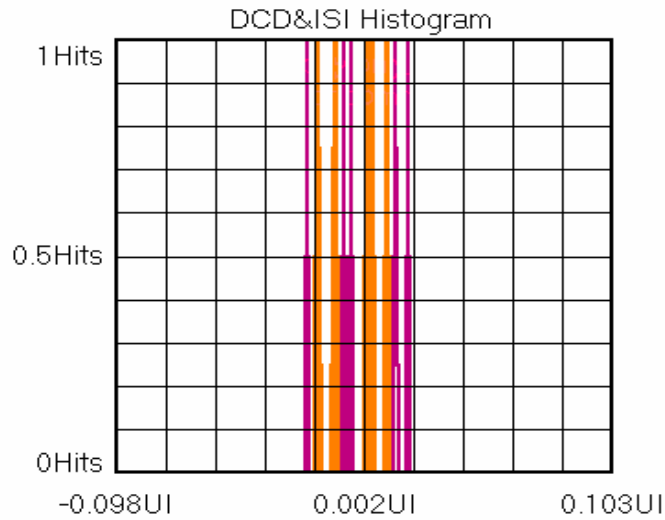


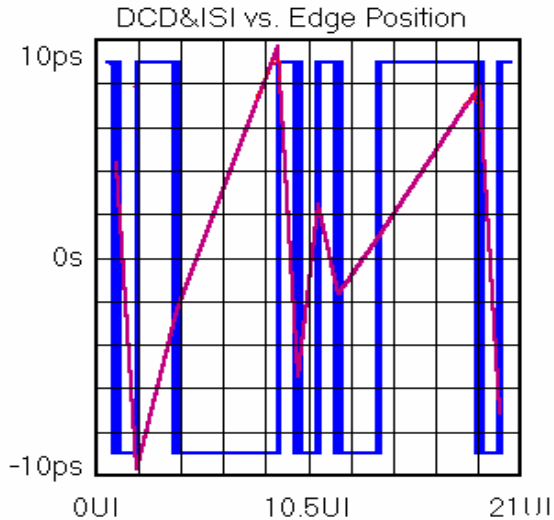
De-Emphasis Induced Jitter Removal (PCIe II)

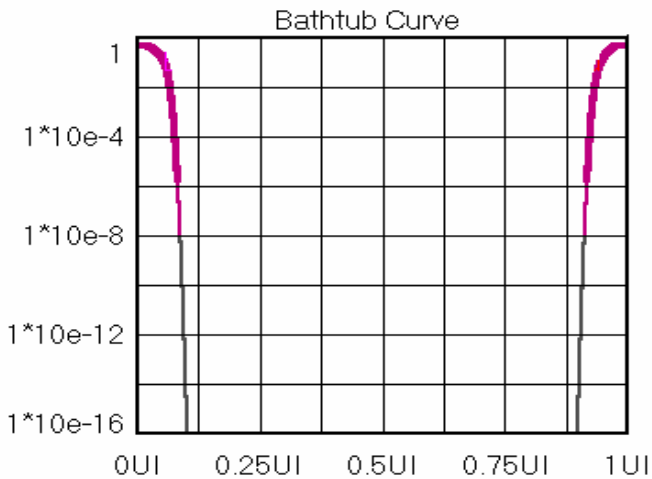


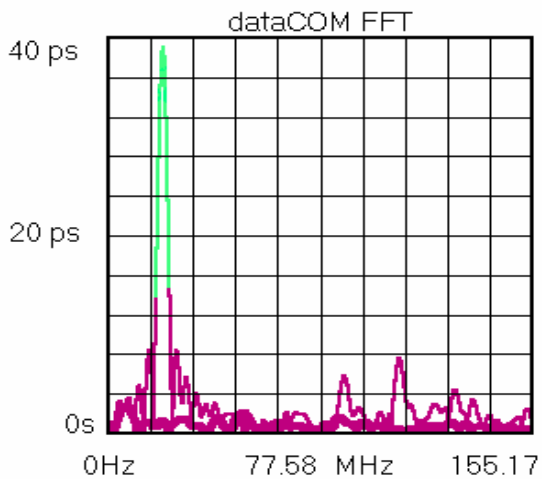


Tx JNB Diagnostic Test Example (PCIe II)

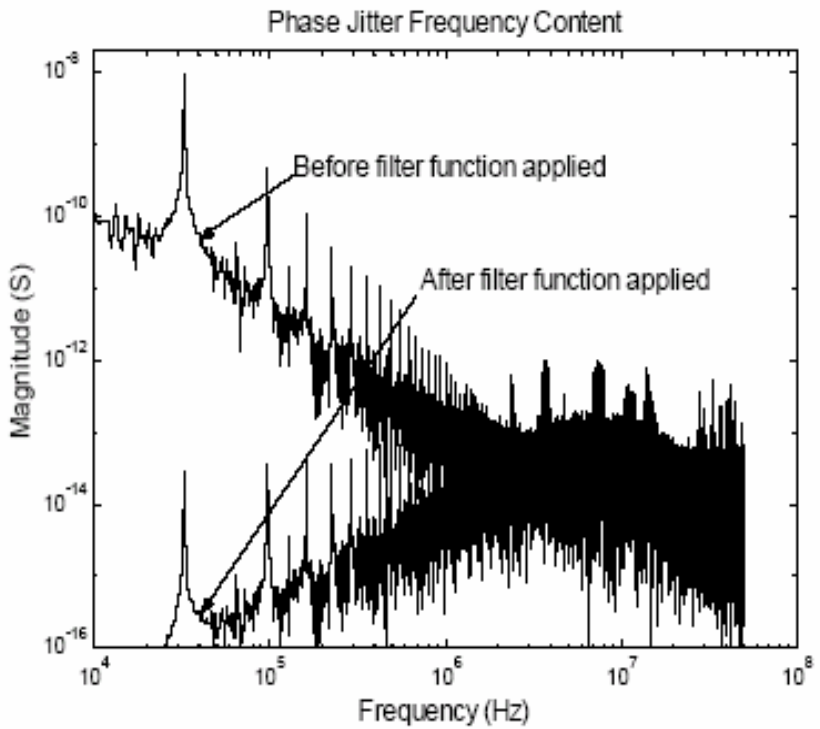


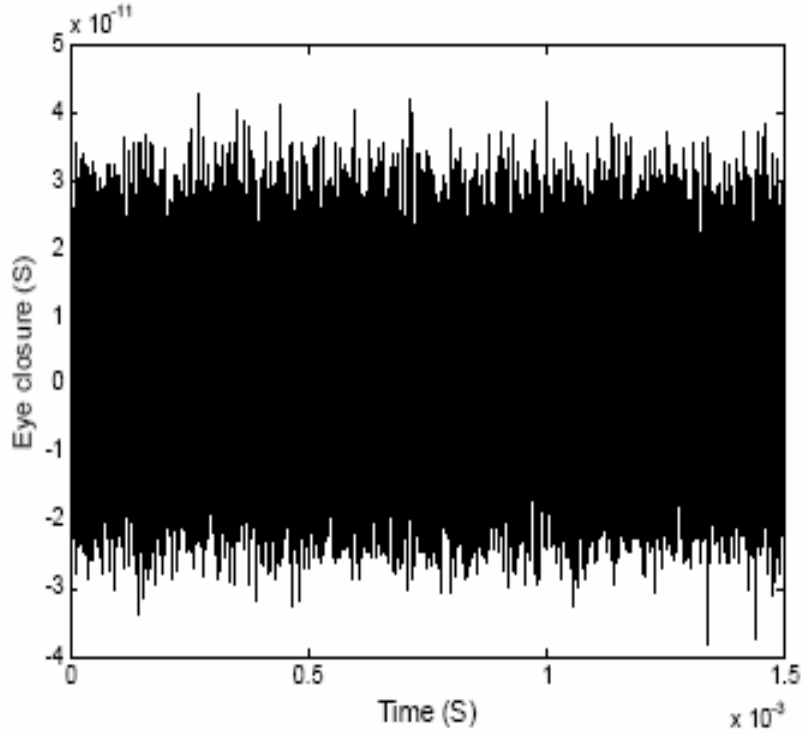






Reference Clock Test Example (PCIe II)

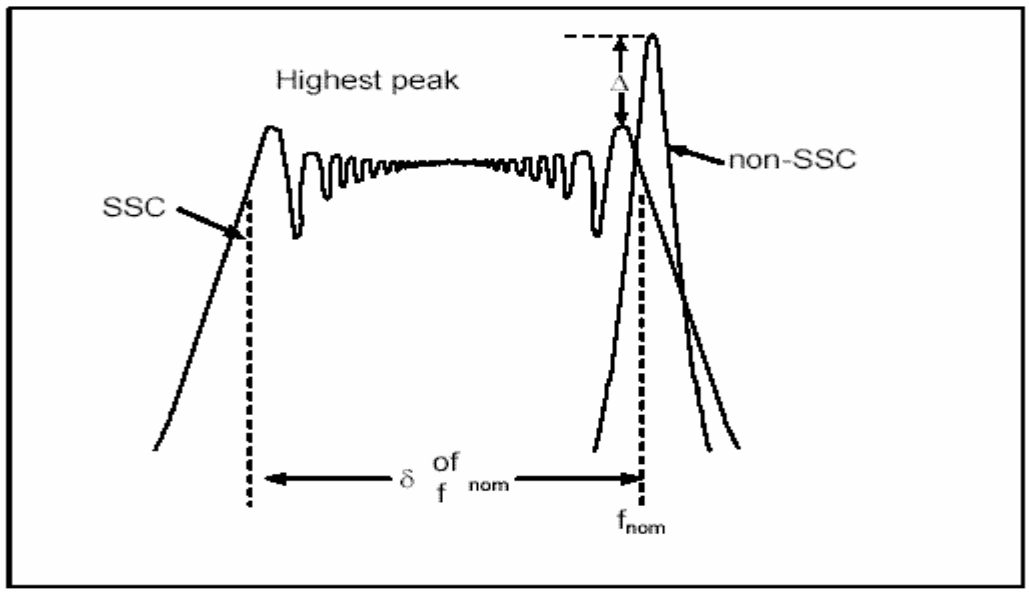




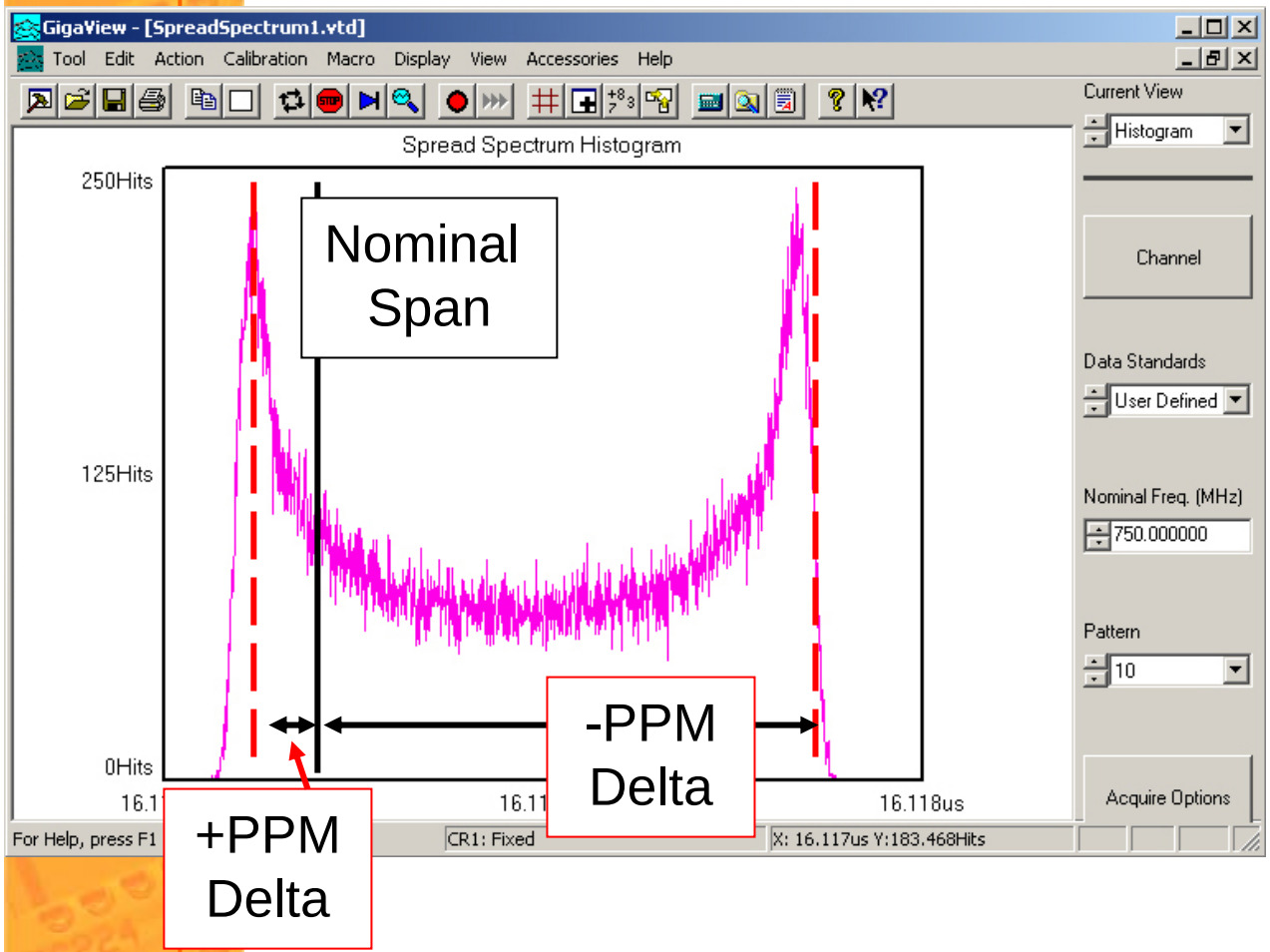
WAVECREST
Be certain of the signal you send.

Spread-Spectrum Clock (SSC) Effects (SATA)

- SSC moves the frequency below nominal
- The SSC induced frequency deviation should be less than ***–5000 PPM (-0.5%)*** below the nominal

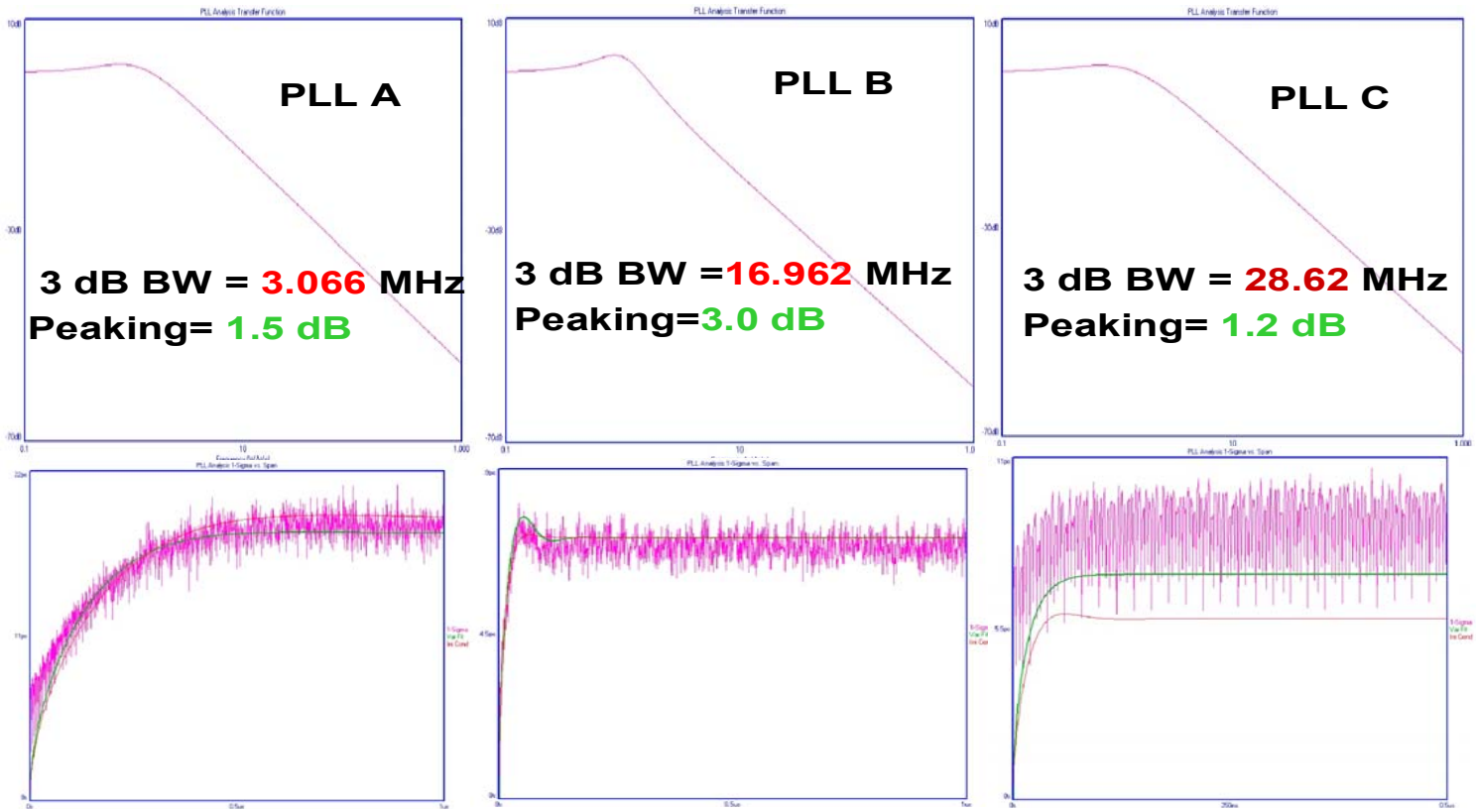


An SATA SSC Measurement

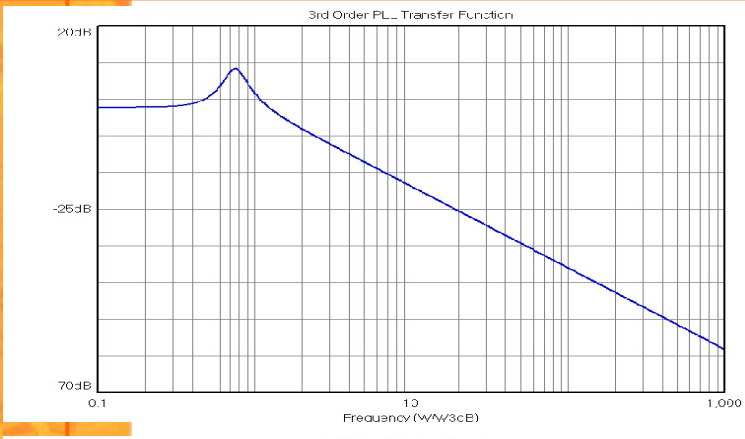


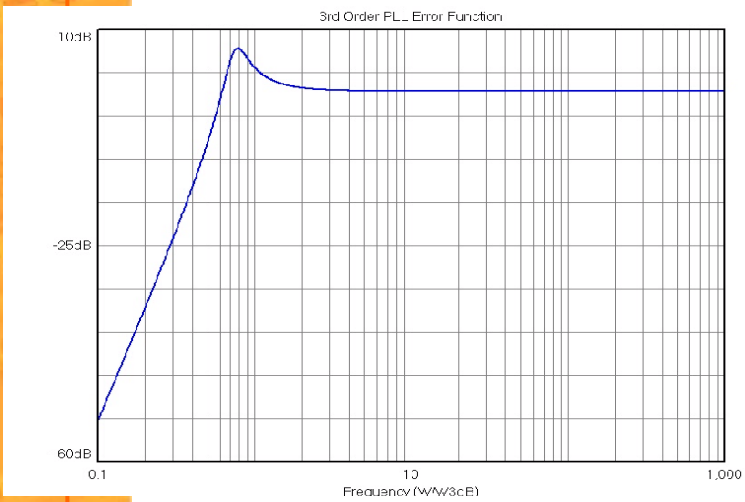
- 1010 Data Required
- Measures across ½ SSC cycle
- Directly measures the Time Domain Deviation due to SSC
- Results in PPM referenced to a nominal span

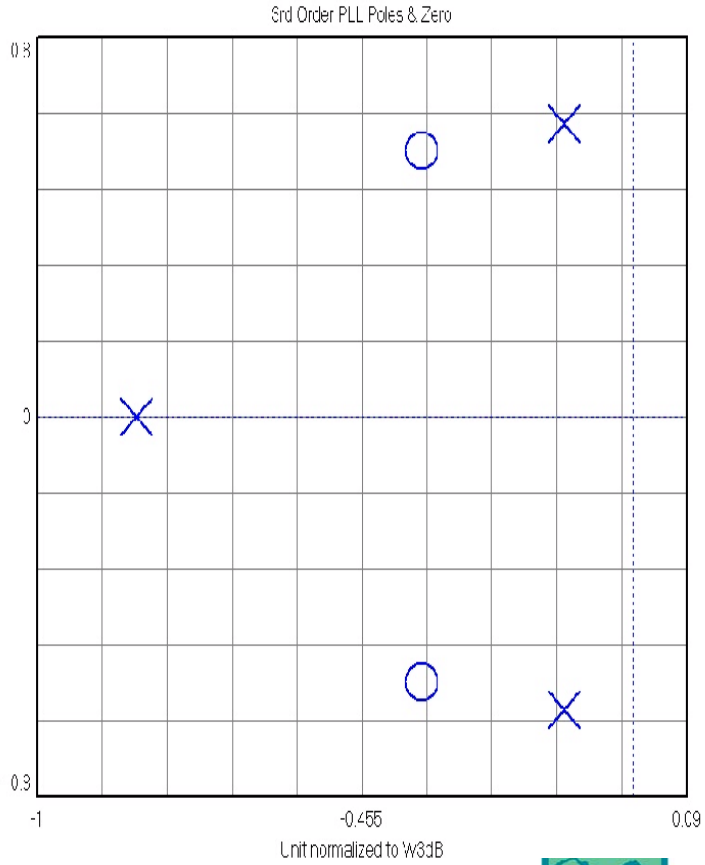
PLL Test Examples (PCIe II)



3rd Order PLL Test Capability (NEW !!!)







WAVECREST
Be certain of the signal you send.

Equipment Used

New Wavecrest SIA 4000 (Spec subject to improve):

- **13 Gb/s** data rate, **15 GHz** bandwidth
- Jitter noise floor < **400 fs** rms
- Rise time: **20 ps**
- **10** SE/DIFF built-in channels, extendable to **32, 64, 128, 256**… etc. via relay matrix
- **< 50-100 ms** throughput per channel for most of the SERDES compliance tests
- Easy integration to ATE system for HVM test.

SIA 4000

WAVECREST
Be certain of the signal you send.

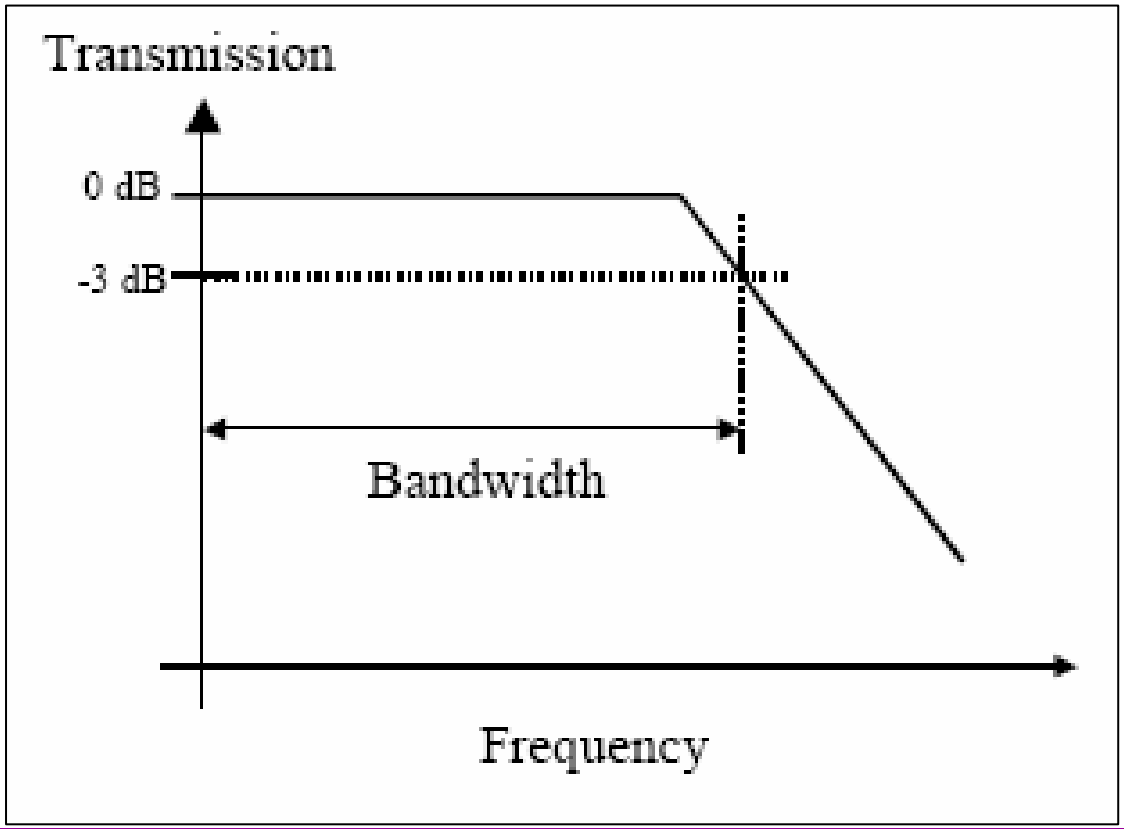
VI. Signal Integrity and Jitter for Test Instrumentation

Evaluating Your Test Equipment Performance

WAVECREST
Be certain of the signal you send.

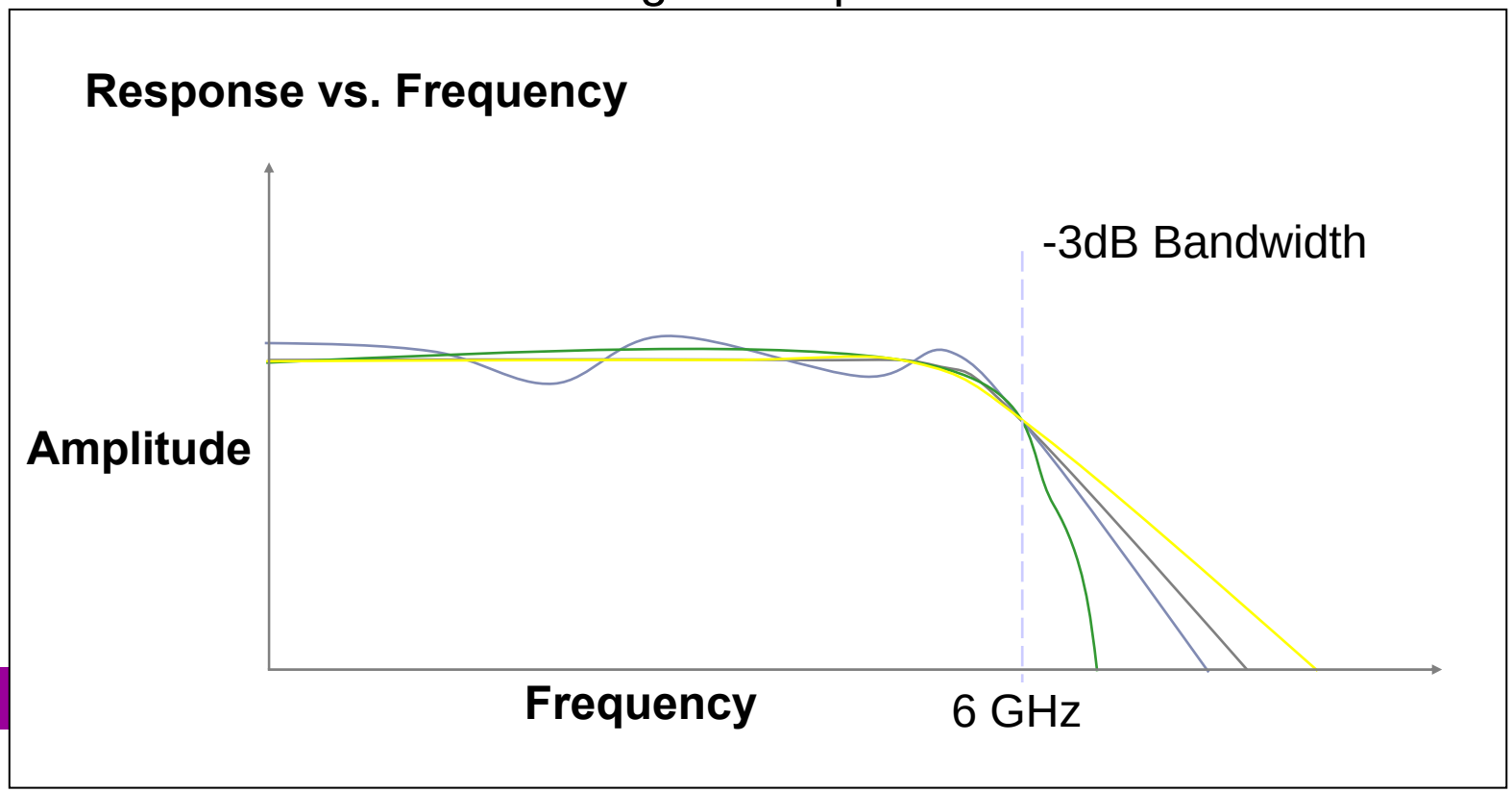
Is Bandwidth a Good Metric for Determining Instrument Performance?

Should a time domain instrument be specified in the frequency domain?

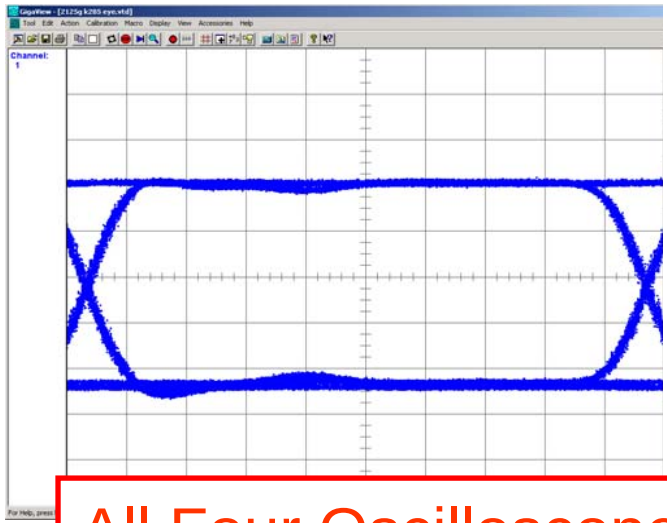


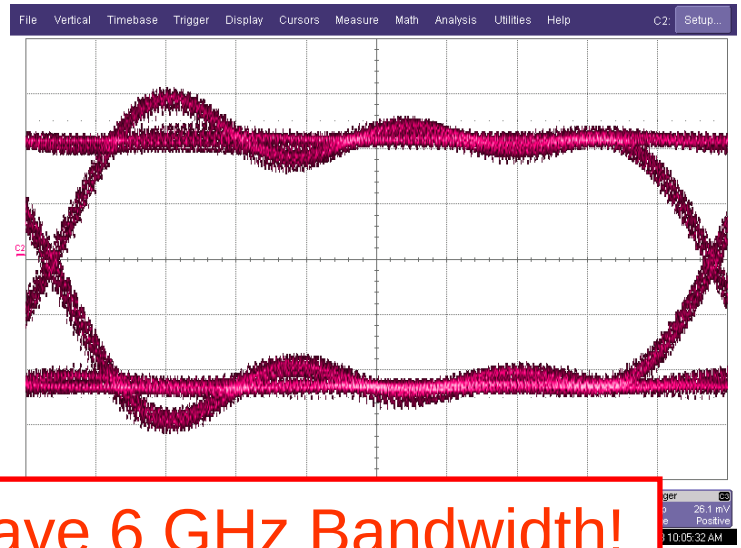
Why Analog Bandwidth is a Poor Metric for Determining System Performance

- Analog bandwidth is only one data point
- It ignores the shape of the response of the system
  - Non-linearity in the response
  - Rate of roll off for higher frequencies

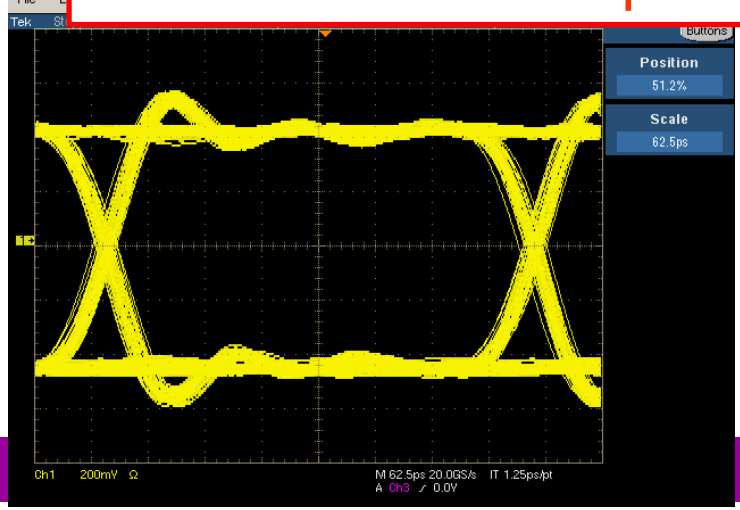


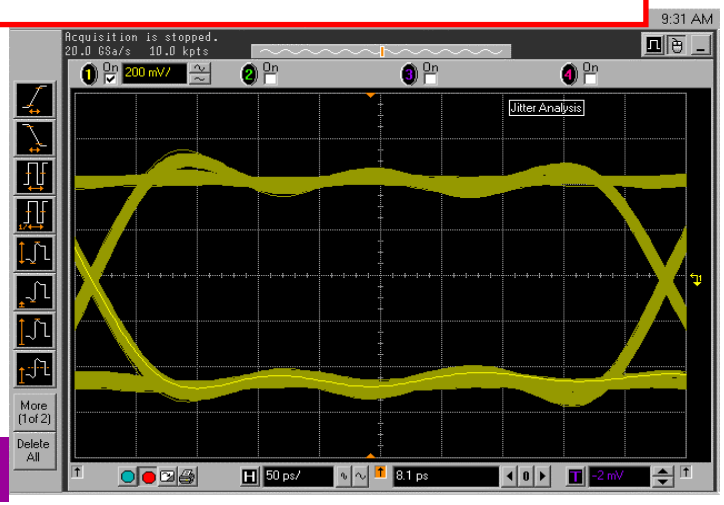
Four Different Oscilloscopes Analyze the Same 2.125 Gb/s Signal



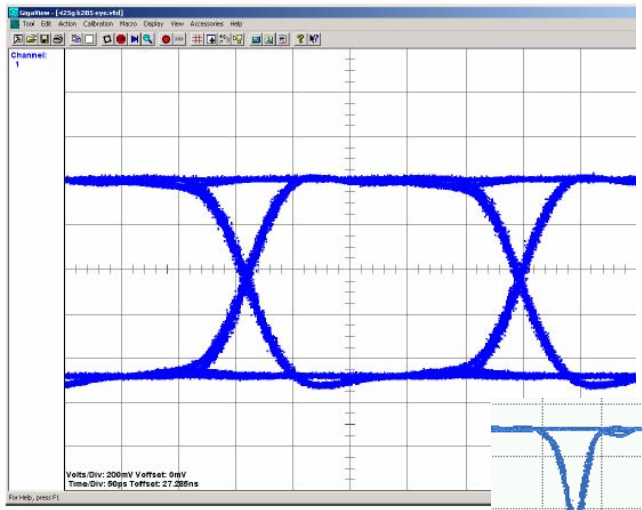


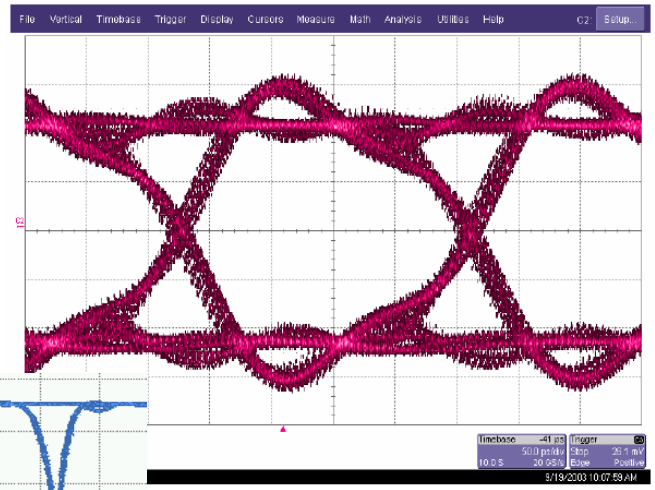
All Four Oscilloscopes have 6 GHz Bandwidth!

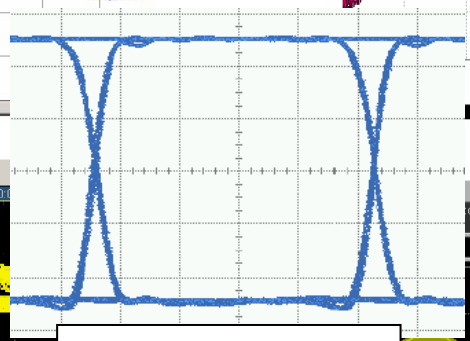


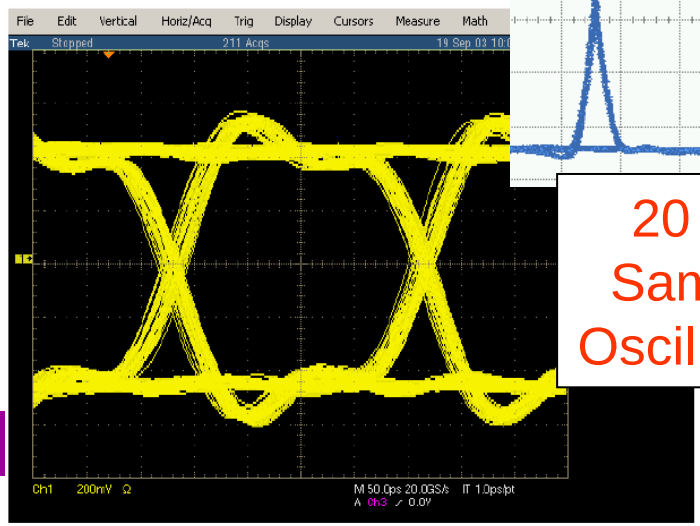


Four Different 6 GHz Oscilloscopes Analyze the Same 4.25 Gb/s Signal

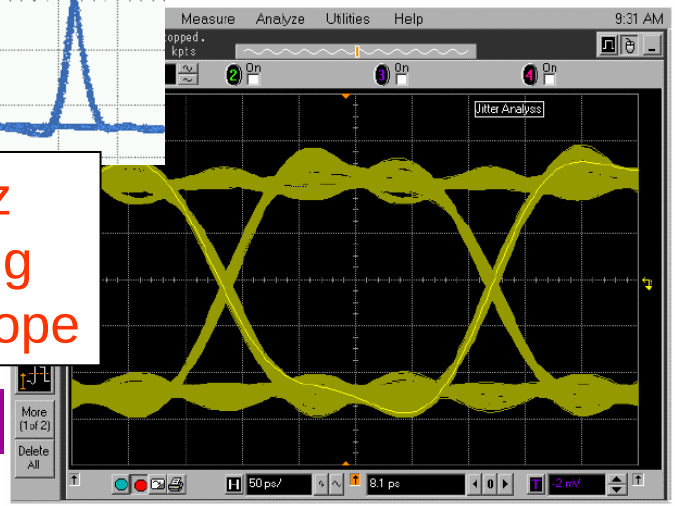




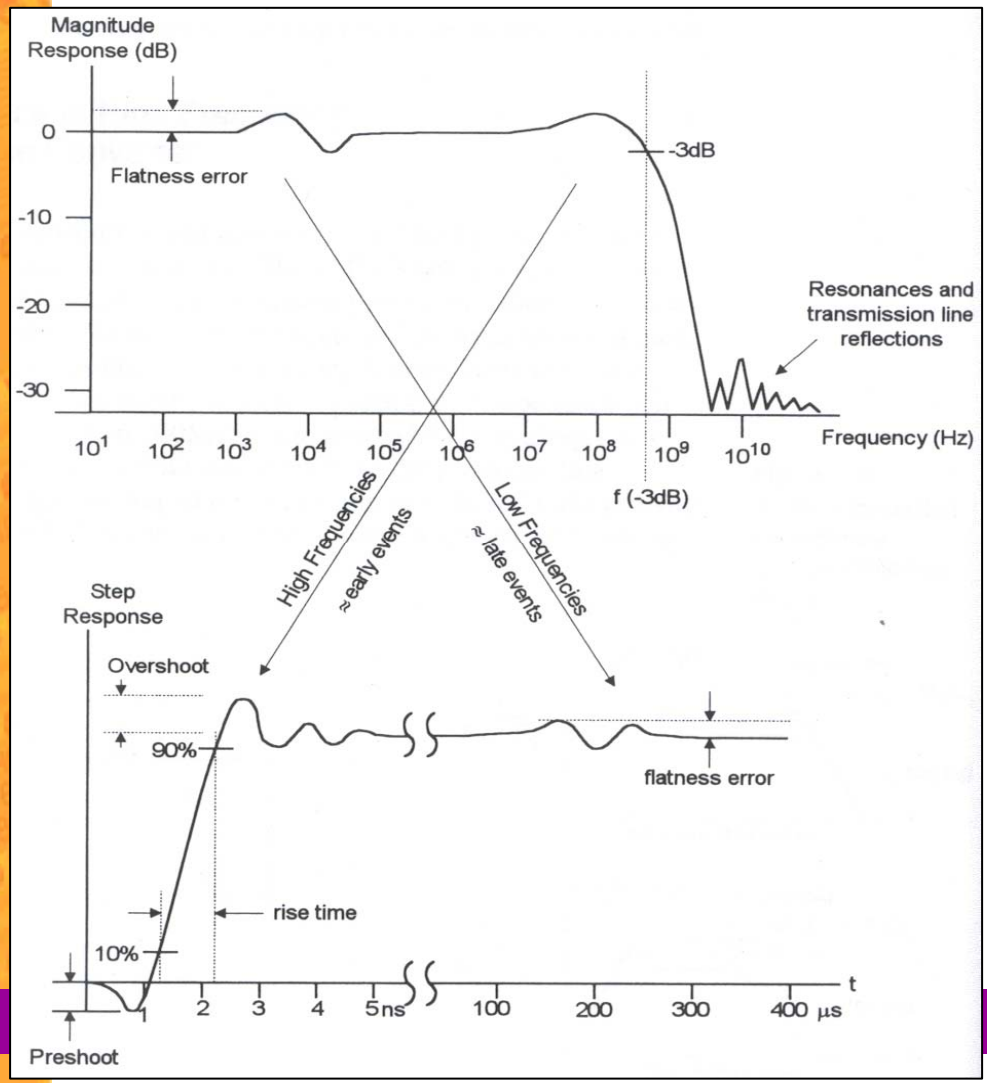




20 GHz Sampling Oscilloscope

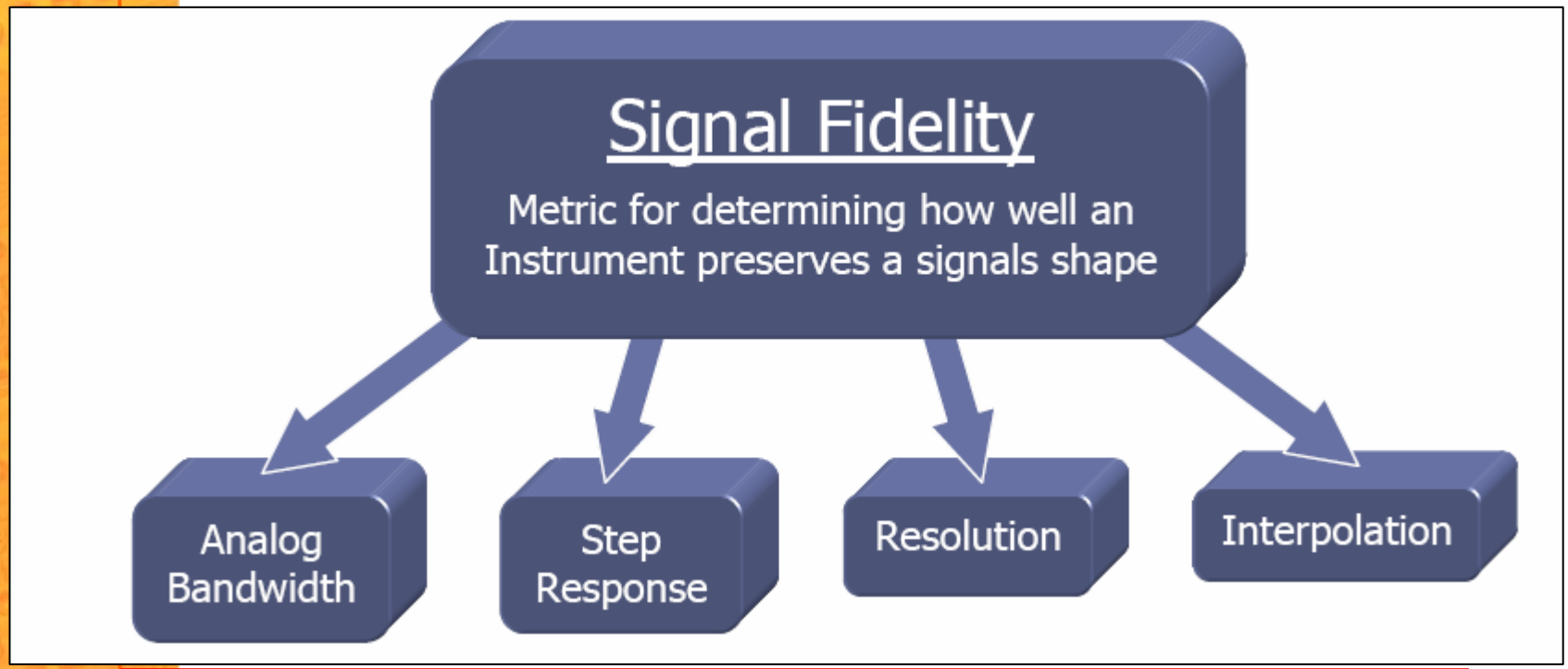


Relationship between Frequency Magnitude and Step Response



Consider how the test instrument responds to a step or fast edge in order to evaluate its performance

Bandwidth is NOT the Only Metric for Determining Instrument Performance



Evaluate the test instrument in your application and compare it to a known standard

What Does this Mean?

- Analog bandwidth along is not sufficient for determining system performance
- These errors result in *failing good parts, lower device margins and poor quality control.*

VII. Summary

- Jitter components provide clues/guides for the root causes and the foundation for statistical extrapolation
- Quantifying RJ and DJ and other sub-components is essential when TJ is tested @ BER=10^{-12} or smaller
- Understanding different jitter measure types is critical
- Transfer function is a must for testing serial links
- JNB needs to be treated as a statistical signal
- General high speed link test methods including Fibre Channel, SAS, PCI Express, FB DIMM, and SATA are illustrated
- JNB and signaling test for major multiple Gbps link are reviewed covering Fibre Channel, SAS, PCI Express, FB DIMM, SATA, etc.
- Case study examples are illustrated and can be applied to related high-speed link tests