Applying signal analysis theory to clock and PLL specifications

By

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This is a presentation to the JEDEC JC-40 committee

WAVECREST

Contents:

- What is “Signal Integrity” with respect to clocks?
  - What is Jitter with respect to clocks on motherboards?
  - What is a Probability density function(PDF)
- The accurate way to measure short cycle and skew jitter. . . together
- What PLL specifications are needed for PC systems
  - PLL response specifications. . .
  - PLL jitter performance specifications. . .
- References. . .
  - IEEE computer society, ITC99 paper 30.2.
  - ANSI, NCITS, T11.2 / Project / 1230 / Rev 10, Annex A.
  - Wavecrest “Jitter Analysis 101” seminar document.

What is Jitter?

- *Hi Frequency deviation from the ideal timing of an event. Jitter is a period / frequency displacement of a signal from its ideal location.*
- *These displacements can occur in amplitude, phase, pulse width, and are generally categorized as either deterministic, or random in nature.*

“Signal Integrity”

“As Clock & Data speeds approach the gigaHertz and gigabit rates, how does the IC manufacturer guarantee 1 year of error free operation to NCITS specifications . . . In a 1 second test?”

What’s at stake . . . “Interoperability”

“Peak to Peak” is not adequate. . .

- It’s impossible to know if you’ve measured the worse case timing uncertainty for an event, Consequently. . .
- It’s necessary to characterize the jitter characteristics of the events in question and separate the Deterministic and Gaussian components to derive a “Clock or Data Error Rate” from the “Probability Density Function” of the parameter your measuring.

“Signal Integrity”

(from Fibre Channel Specification)

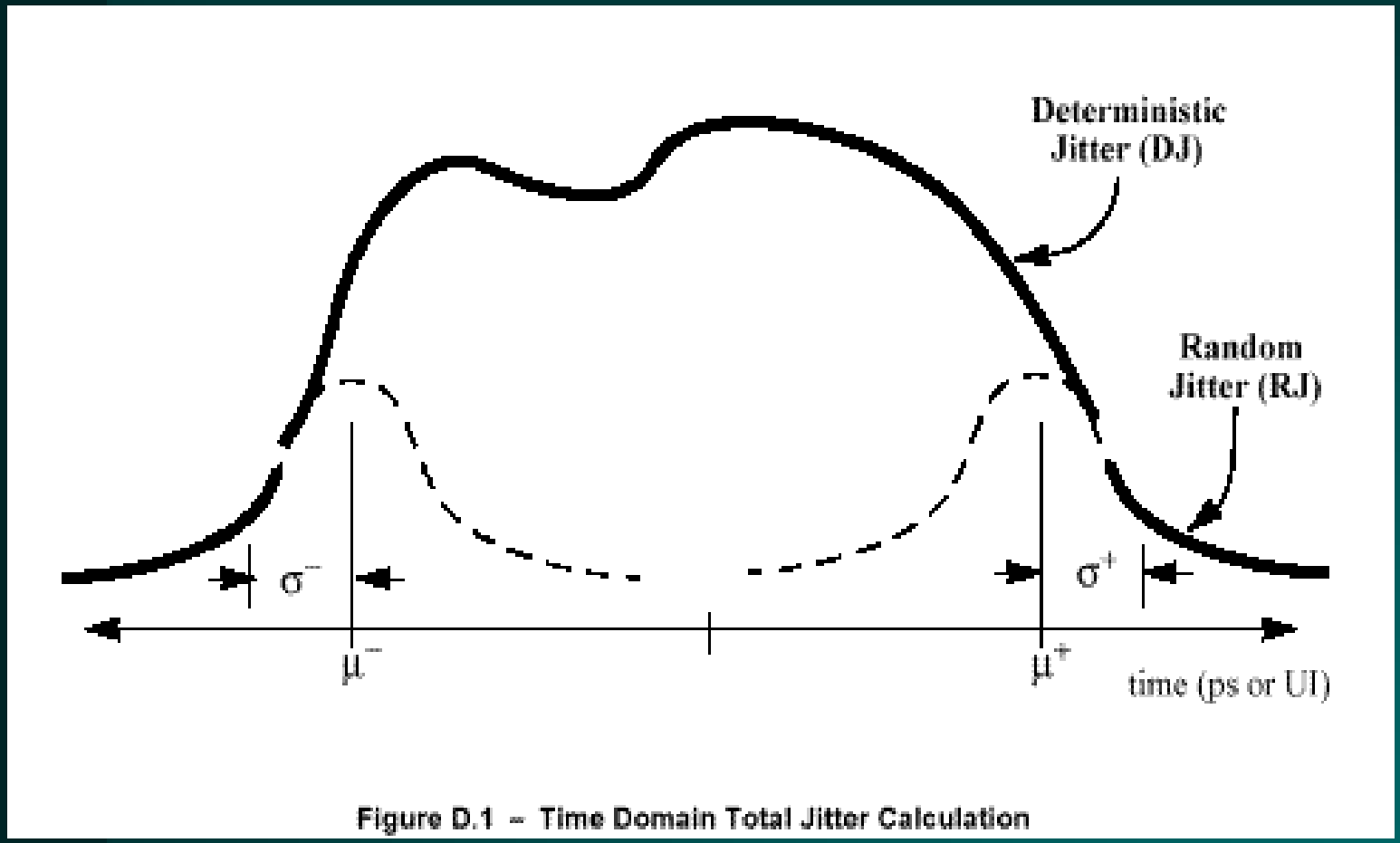
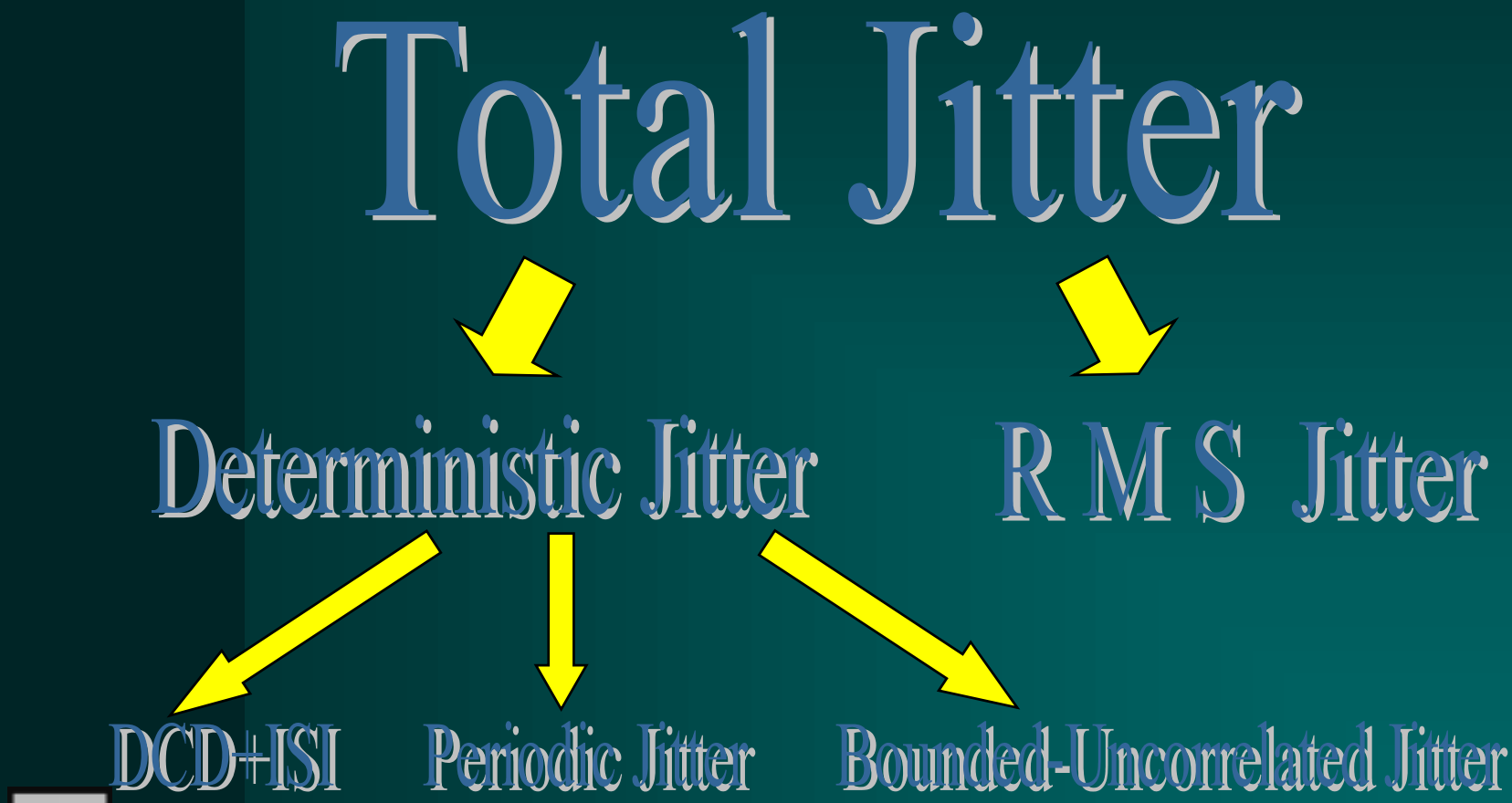


Figure D.1 – Time Domain Total Jitter Calculation

Signal Integrity breakdown



Total Jitter is made up of various components. . .

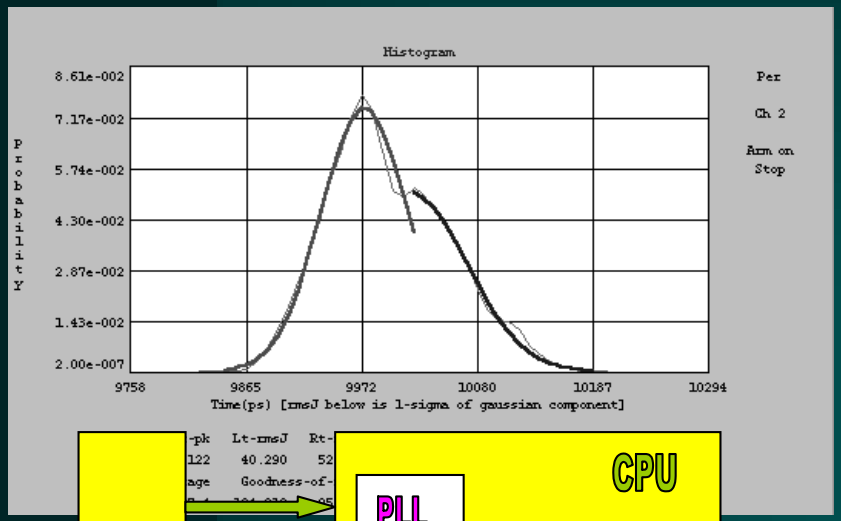
- Deterministic components. . . Bounded jitter
  - Periodic jitter (Pj)
  - Duty cycle distortion (DCD)
  - Data dependent jitter (DDj)
  - Inter symbol interference (ISI)
  - Bounded uncorrelated jitter (Buj)
- Random component (rmsj). . . Unbounded jitter
  - Gaussian component is the long term failure mechanism.

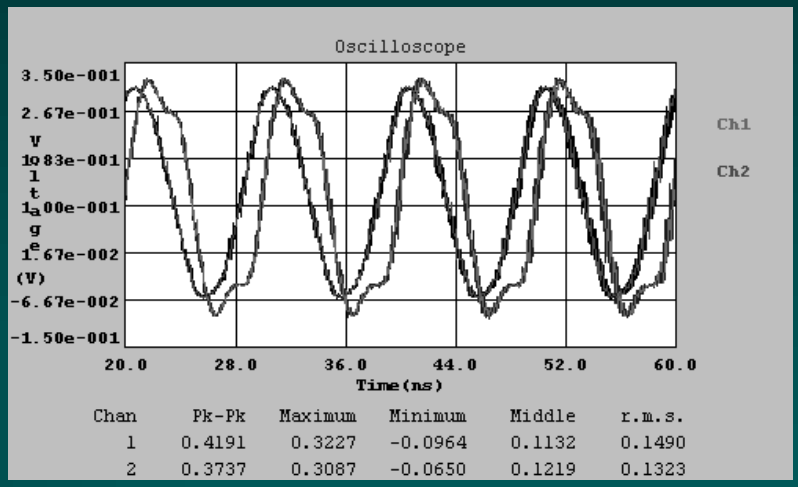
Jitter Analysis

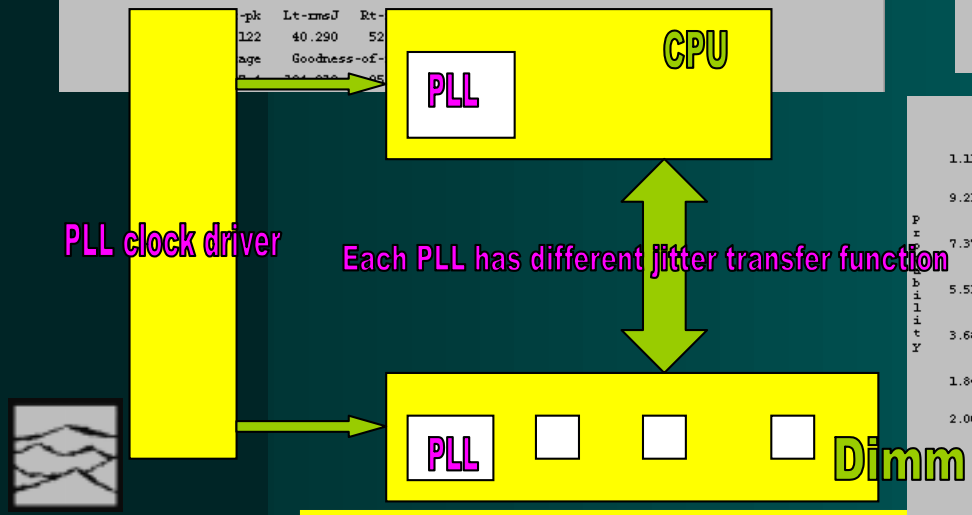
- Jitter
- Jitter Tolerance (Receiver)
- Jitter Generation (Xsmitter)
- Jitter Transfer (Xmit / Rcv)
- Correlated
- Duty Cycle Distortion Jitter
- Data Dependent Jitter
- Non Correlated Jitter (Rndm)
- I / O Jitter
- Period Jitter
- Cycle to Cycle Jitter
- Long Term (Accumulated)
- Low Frequency Jitter
- Jitter Modulation
- High Frequency Jitter
- Jitter Spectrum
- Bit Error Ratio (BER)
- Eye Diagram
- Intersymbol Interference (ISI)

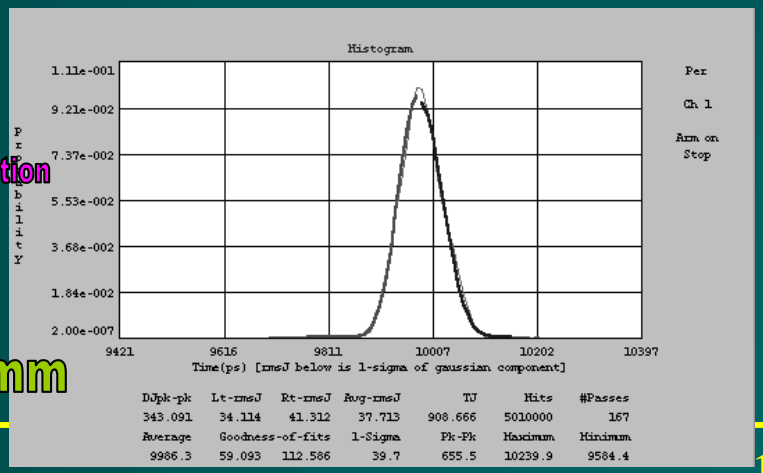
Short cycle + Skew. . .

- Short cycle + path skew in one measurement



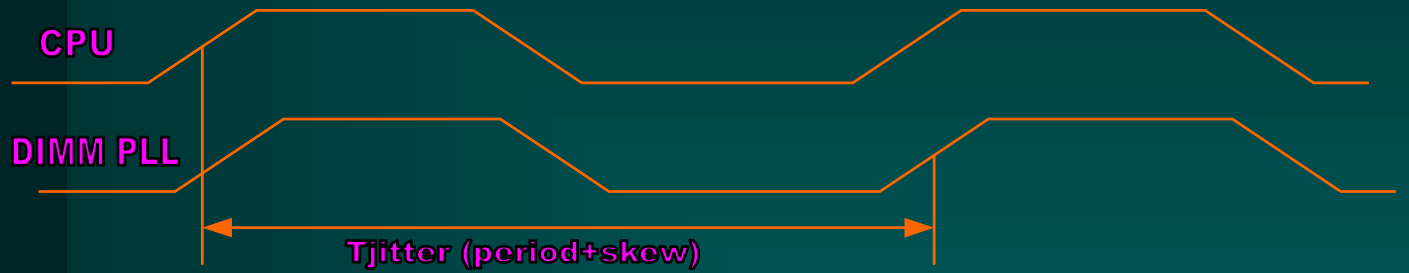


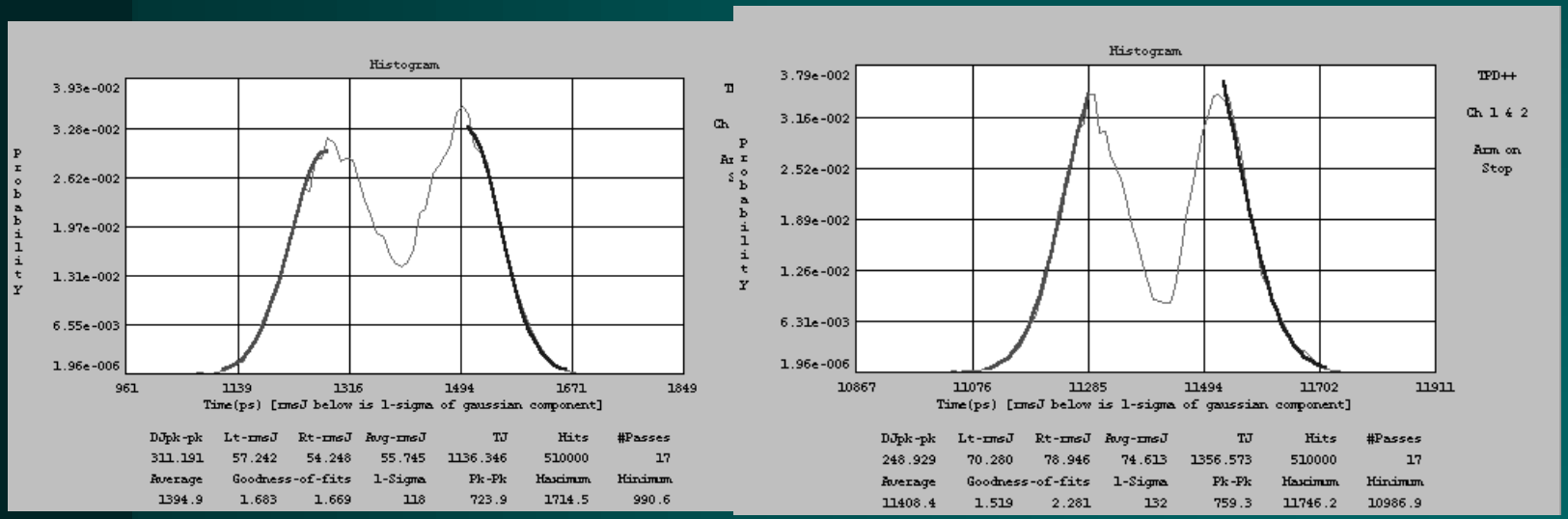




How to measure Period + skew. . .

- Because of the different PLL transfer functions it is necessary to differentially measure the instantaneous time between the CPU clock input and the DIMM PLL clock output. . .





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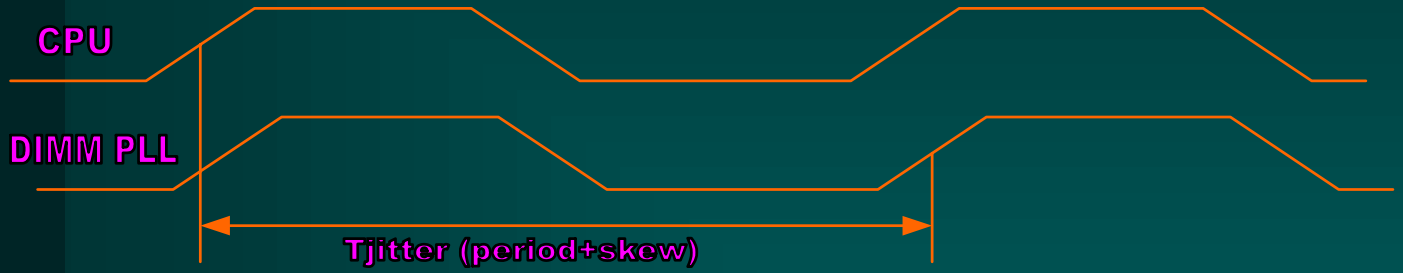

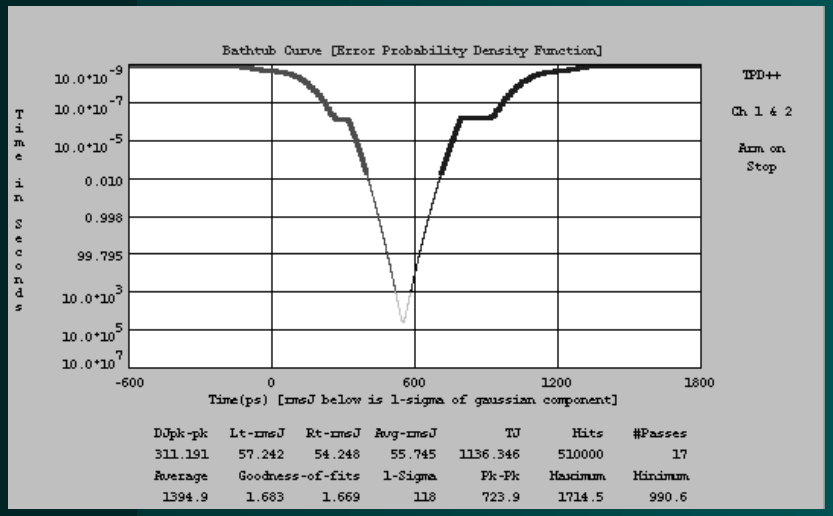

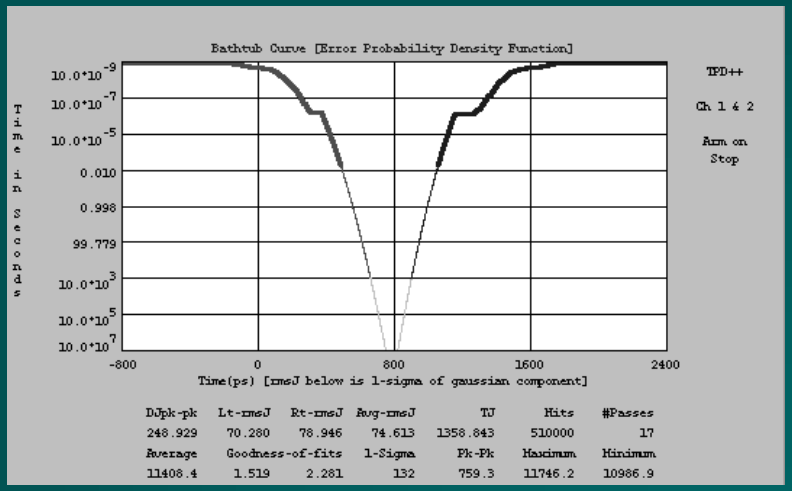

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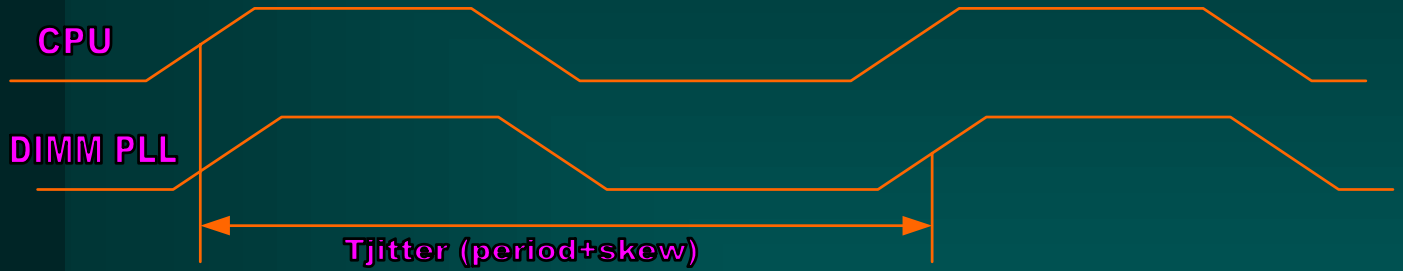

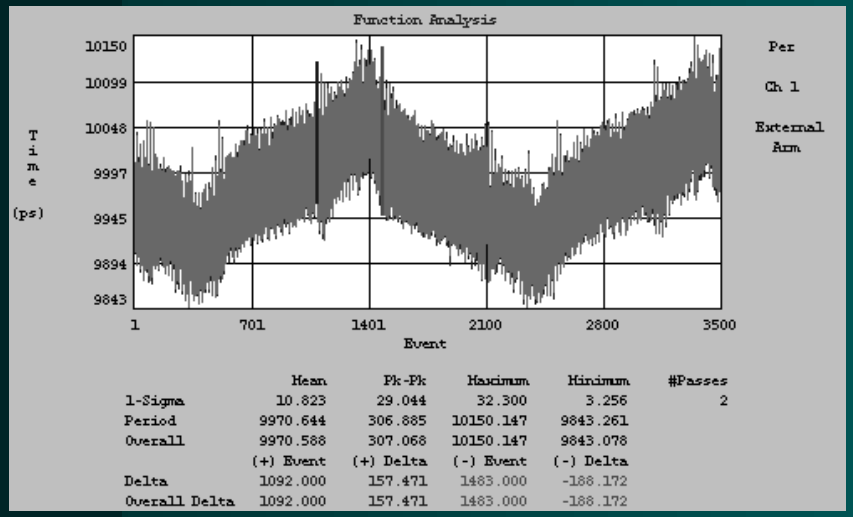

	Mean	Pk-Pk	Maximum	Minimum	#Passes
1-Sigma	10.823	29.044	32.300	3.256	2
Period	9970.644	306.885	10150.147	9843.261	
Overall	9970.588	307.068	10150.147	9843.078	
	(+) Event	(+) Delta	(-) Event	(-) Delta	
Delta	1092.000	157.471	1483.000	-188.172	
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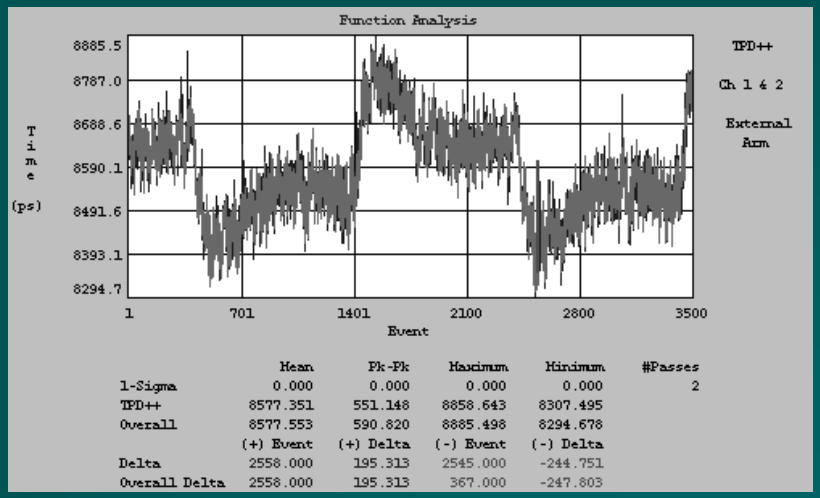
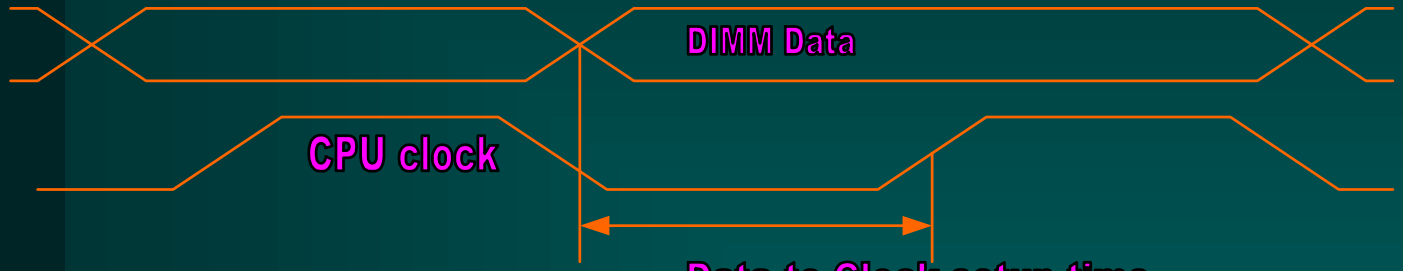
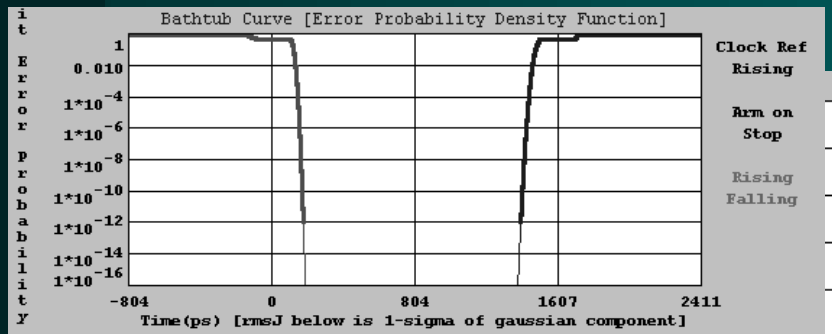


	Mean	Pk-Pk	Maximum	Minimum	#Passes
1-Sigma	0.000	0.000	0.000	0.000	2
TPD++	8577.351	551.148	8858.643	8307.495	
Overall	8577.553	590.820	8885.498	8294.678	
	(+) Event	(+) Delta	(-) Event	(-) Delta	
Delta	2558.000	195.313	2545.000	-244.751	
Overall Delta	2558.000	195.313	367.000	-247.803	

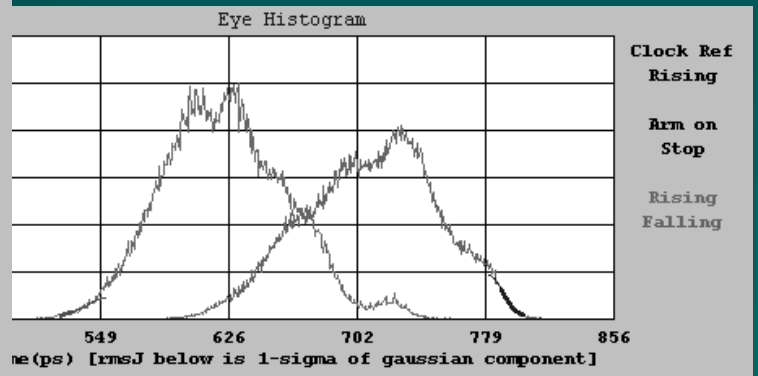
Clock to Data Jitter. . .

- Because the DIMM Data has a transfer function which is different than the CPU clocks PLL transfer function, it is necessary to measure the actual clock to data setup and hold times. . .





	DJpk-pk	Lt-rmsJ	Rt-rmsJ	Avg-rmsJ	TJ	PK-PK	1-SIGMA
Data	227.374	13.488	8.967	11.227	383.539	301.5	57.704
Clock	51.091	12.643	15.513	14.078	247.195	166.6	31.168
		Lt-ChiSq	Rt-ChiSq	Hits	UI	Ck-Data skew	
Misc		0.832	0.719	264593	1607.272	667.762	



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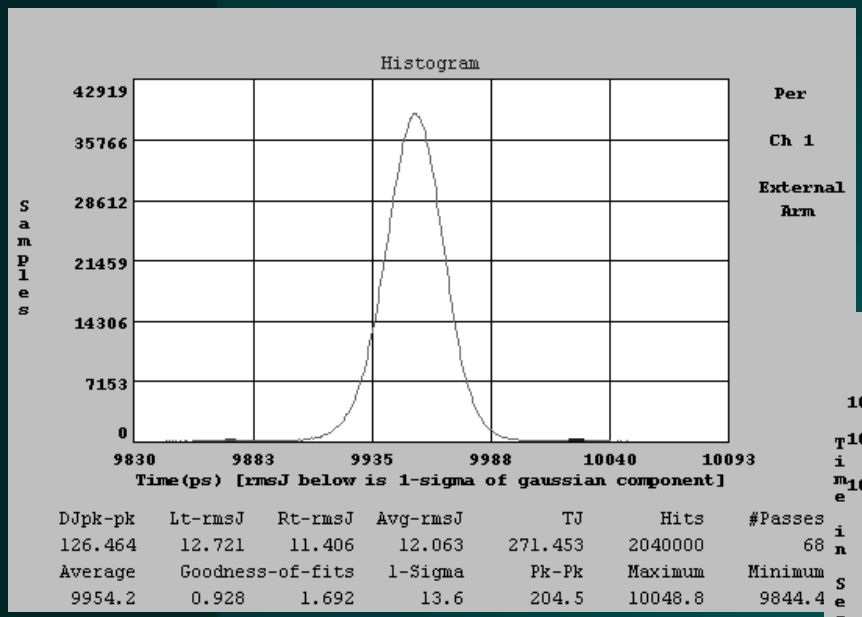
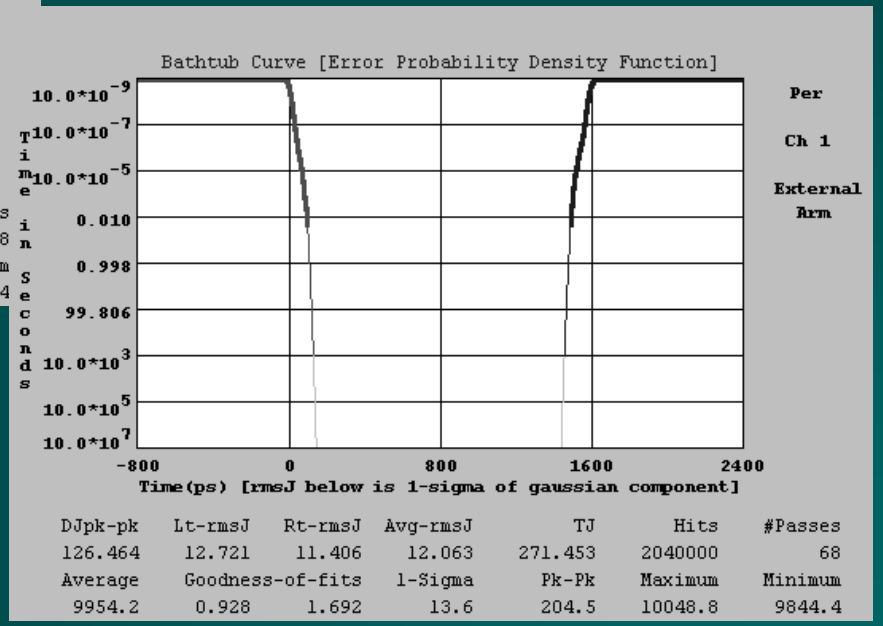
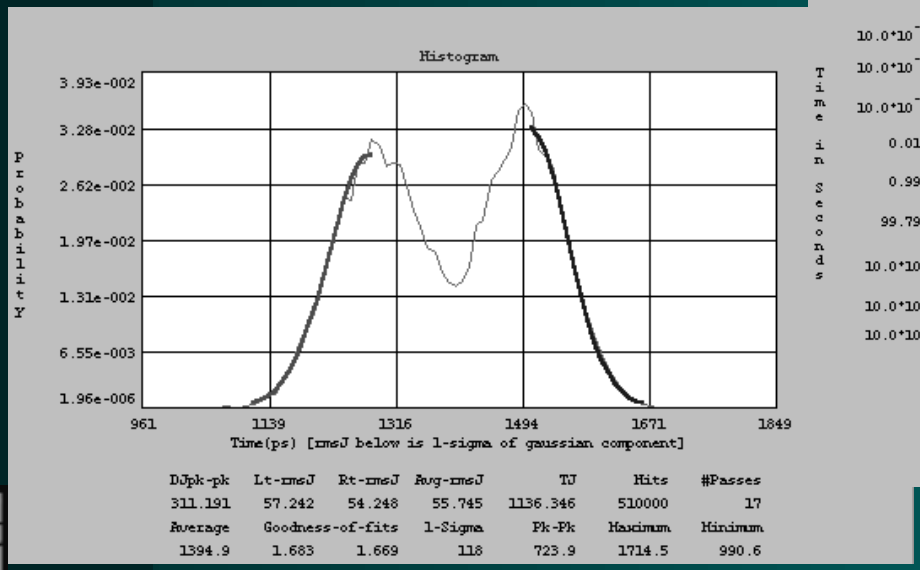
"By characterizing the JITTER components you can accurately estimate the long term reliability of any signal ." (Reference ANSI . . . MJS document.)

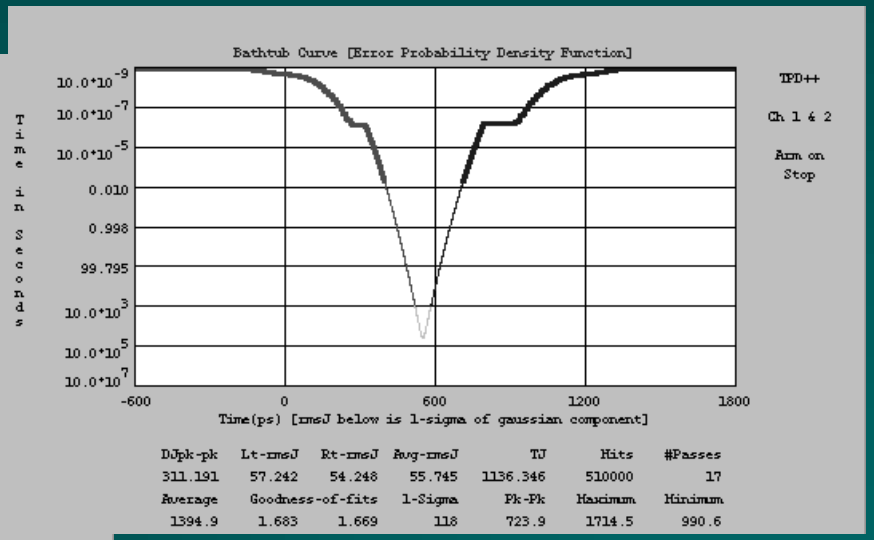




Applying PDF to results. . .

- Generate Total Jitter specifications based on a specified "Probability of Failure" value. . . 10e-12 for example. This approach eliminates inherent errors of Pk-Pk specifications.
- The simplified formula for Total Jitter:
  - Tj is equal to Dj + (rmsj * sigma). Conservative estimate.
  - The probability density function of the measured distribution gives a more accurate estimate of the failure rate.



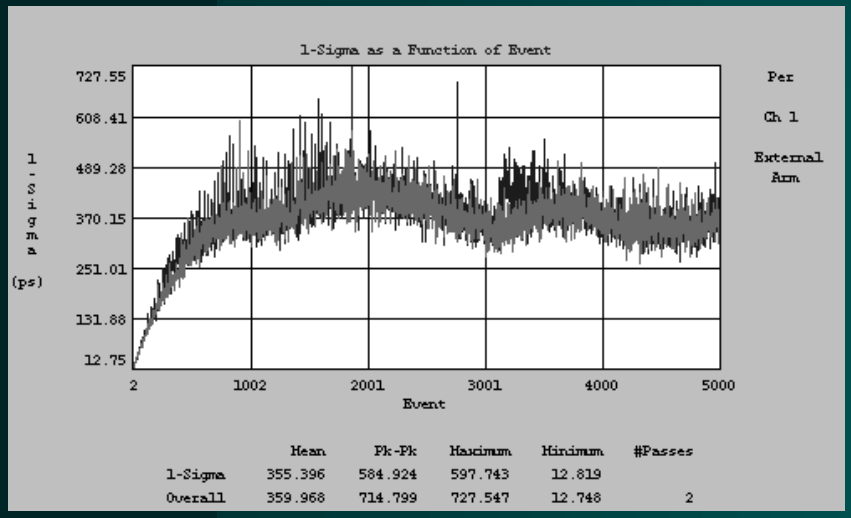


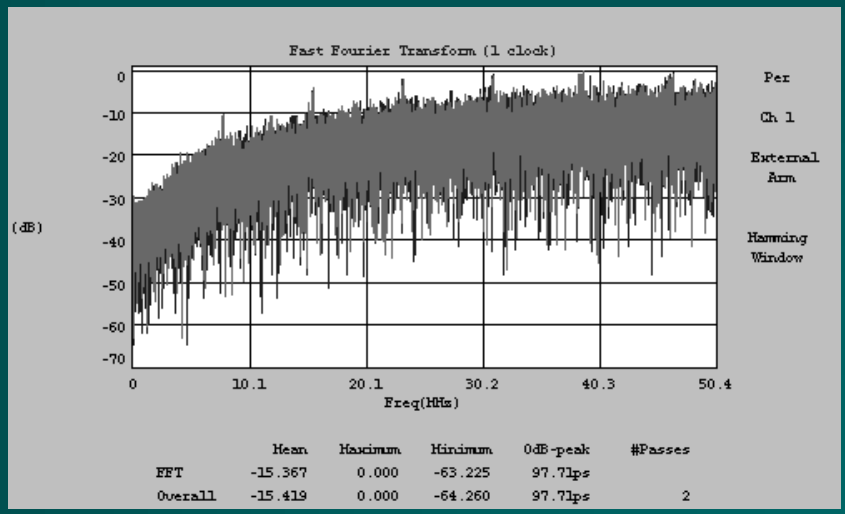
PLL specifications

- PLL loop transfer function
- PLL damping factor & natural frequency (or loop bandwidth)
- PLL jitter transfer (external jitter effects)
- PLL Jitter Tolerance
- PLL jitter generation (internal jitter effects)

PLL Response. . .

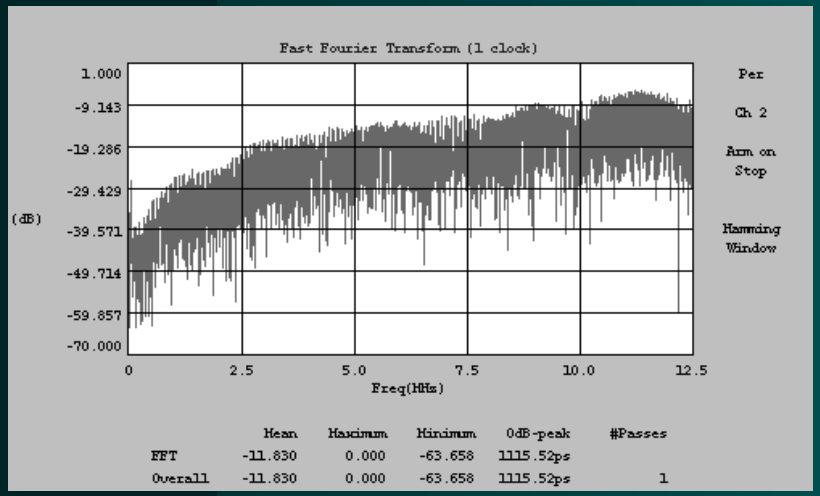
- Loop transfer function. . .
- Damping factor and natural frequency (or loop bandwidth)
- To guarantee minimal jitter transfer when cascading PLL's
- To guarantee repeatable jitter generation or RJ specifications.

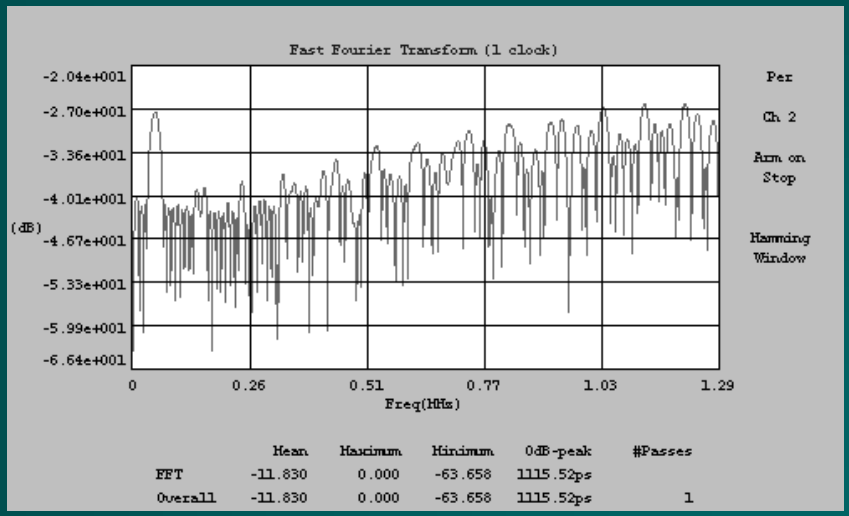




PLL Response. . .

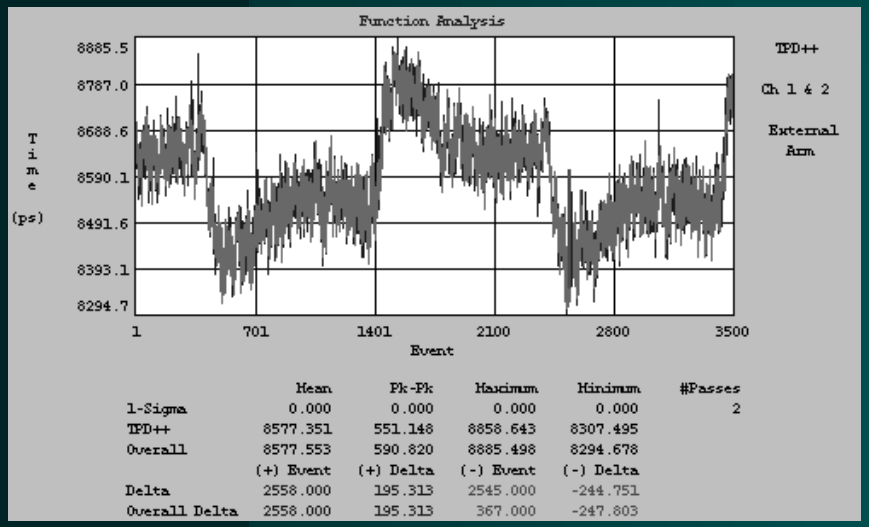
- Loop transfer function. . . With spread spectrum. . .
- Damping factor and natural frequency (or loop bandwidth)
- To guarantee minimal jitter transfer when cascading PLL's
- To accurately measure spread spectrum modulation contribution to short cycle specifications.





PLL Response. . .

- Loop transfer function. . .
- Damping factor and natural frequency (or loop bandwidth)
- To guarantee minimal jitter transfer when cascading PLL's
- To account for Mother Board layout and noise problems.



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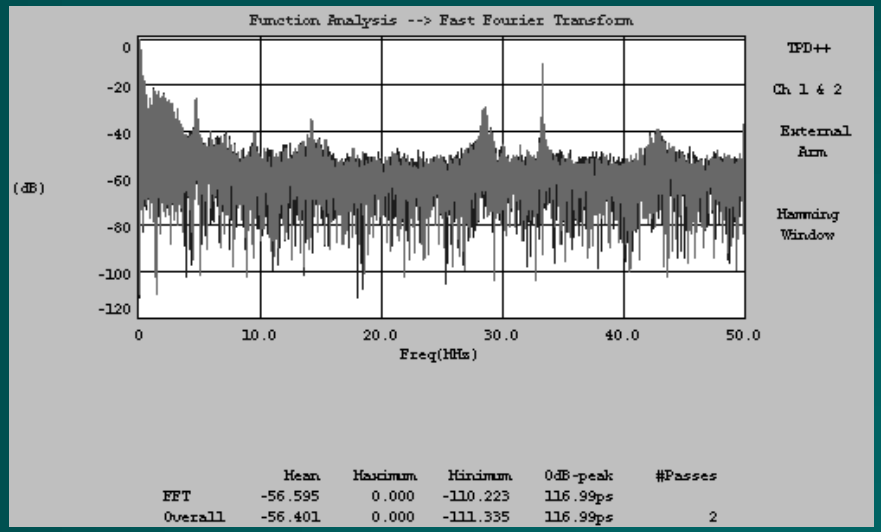
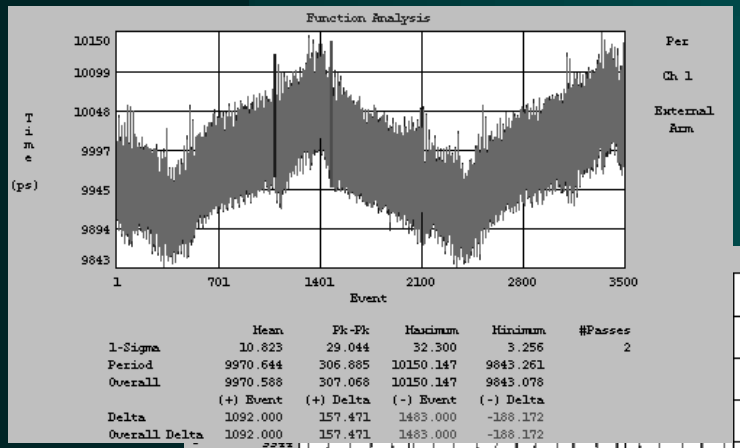


	Mean	Maximum	Minimum	0dB-peak	#Passes
FFT	-56.595	0.000	-110.223	116.99ps	
Overall	-56.401	0.000	-111.335	116.99ps	2

PLL Response. . .

- Loop transfer function. . .
- Damping factor and natural frequency (or loop bandwidth)
- To guarantee minimal jitter generation when cascading PLL's
- The main jitter contributor here is the PLL's charge pump.



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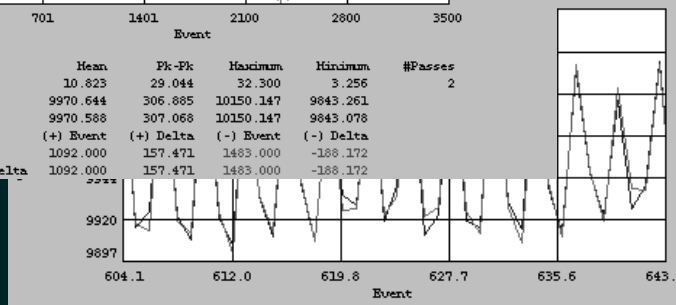

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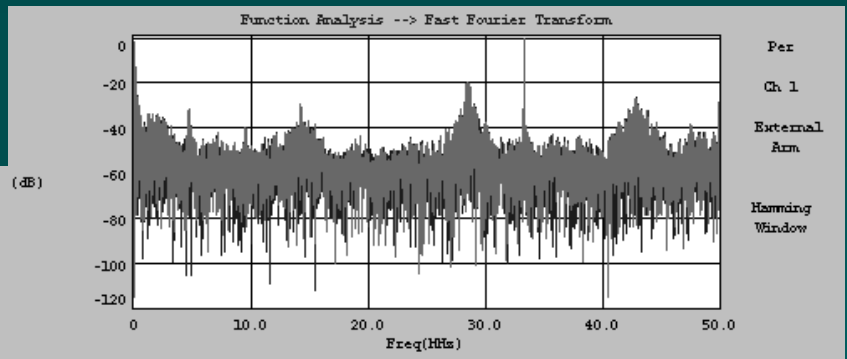
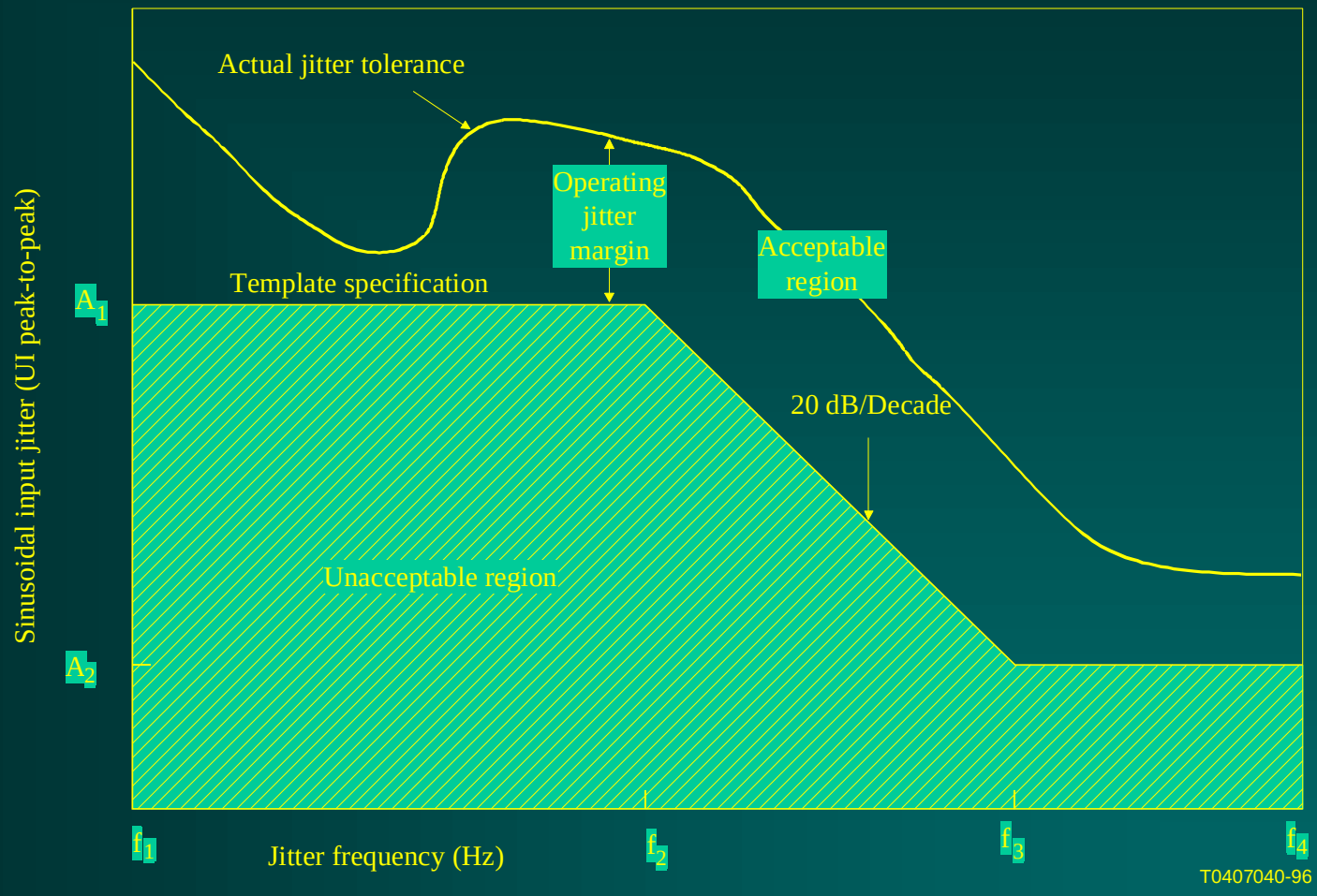
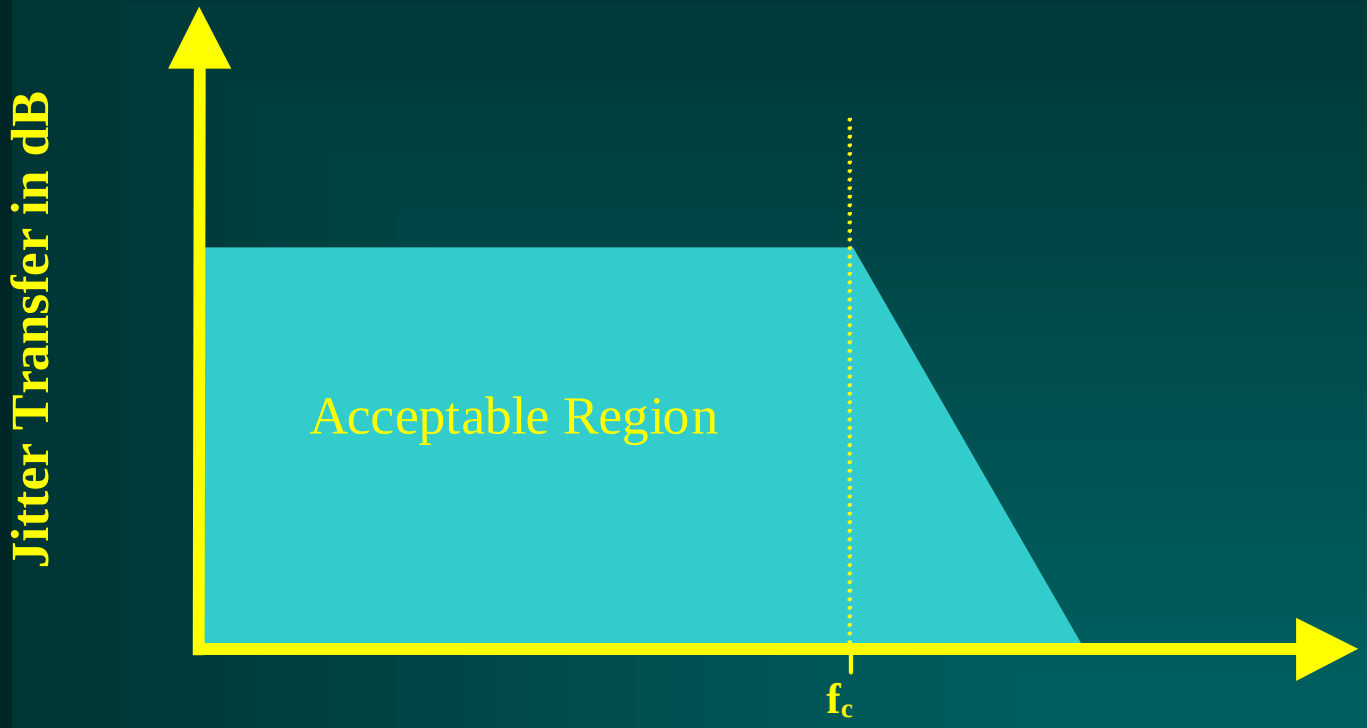


	Mean	Maximum	Minimum	0dB-peak	#Passes
FFT	-55.170	0.000	-115.474	59.89ps	
Overall	-55.280	0.000	-115.474	60.13ps	2

Jitter Tolerance



Jitter Transfer



The next step to higher speeds. . .

- Adopt the NCITS pdf model for total timing uncertainty (TJ) for all specifications in place of the current pk-pk nomenclature.
- Add “Period + Skew” measurement criteria to EIA / JESD65 specifications.
- Add “Data to Clock” measurement criteria to EIA / JESD65 specifications.
- Add PLL response specifications to EIA / JESD65 specifications.

References. . .

- ANSI / NCITS T11.2 / Project 1230 / rev 10, Annex A.
- IEEE Computer Society ITC99 paper 30.2 “A New Method of Jitter Decomposition Through It’s Distribution Tail Fitting”.
- Wavecrest Corporation “Jitter Analysis 101” Seminar manual.
- EIA / JESD65 Specifications for standard logic devices.
- Intel AN-333 clock applications note.