tools GigaView Clock Module

PLL Analysis Tool

Verify PLL Design Goals

The use of Phase Lock Loops (PLL) is commonplace in today's communication devices. PLL's are a critical component because they are needed to synchronize an output signal to an input signal. PLL testing using a variety of test instruments such as oscilloscopes, spectrum analyzers, modulation signal generators and pulse generators creates complicated test setups often taking hours to complete a thorough analysis. These limitations are overcome with the GigaView PLL Analysis tool and the SIA Family of Signal Integrity Analysis solutions. PLL's can be completely characterized by the SIA with no other hardware needed. In seconds, you get feedback on device performance. Fast, thorough analysis means fast time to market for your latest innovations.

Quantify PLL Parameters and Transfer Functions

The PLL Analysis tool quantifies the most important PLL parameters and generates plots that provide information about device characteristics and performance. The software determines PLL parameters such as the damping factor, natural frequency, lock range, lock-in time, pull-in time, pullout range, noise bandwidth and power spectral density of the noise. Graphs showing the PLL transfer function, poles and zeros and Bode plot are also generated. Quantifying PLL performance is useful for designers and engineers to determine the performance of their PLL in order to insure that the design goals have been achieved and if there is sufficient margin. As a result, the PLL Analysis tool provides an excellent feedback loop between design goals and actual device performance. In addition, the analysis takes only seconds to complete, enabling more devices to be characterized for a more thorough analysis.

Simple Setup

PLL analysis is performed using one of the SIA Signal Integrity Analysis solutions and GigaView software. The setup consists of connecting the output of the PLL under test to the SIA. No additional test equipment is needed to modulate reference frequency of the PLL under test.

In addition to the PLL, additional signal analysis can be performed using the comprehensive Clock Analysis tool. The Clock Analysis tool quantifies Random Jitter, Deterministic Jitter, the frequency and magnitude of Periodic Jitter, Random Jitter over a bandwidth, Cycle-to-Cycle Jitter, Period and Pulse Width Jitter, rise time, fall time and voltage levels.





Quantify the most important PLL parameters such as:

- Carrier Frequency Damping factor Natural frequency Lock Range Lock-in time Pull-in-time Pull-out-range Noise Bandwidth PSD of the Noise
- Obtain plots for PLLs such as: Transfer Function Bode Plot Poles and Zeros
- Highlights of the PLL Analysis Tool: No modulation signal required Measure transfer function from kHz to Nyquist Measurement requires only the PLL output Fast test time (seconds)
- Requirements for the PLL Analysis Tool: 2nd or 3rd order PLL Low noise PLL reference clock No periodic jitter on PLL output



Raw data obtained from a PLL showing the I sigma versus time span and the model based curve fit (solid line) that is used to derive the PLL parameters.



Transfer function of the PLL normalized to the natural frequency. The peaking of 7 dB in the transfer function shows that the response is oscillatory and damped characteristic with a damping factor <1.

Carrier Frequency	145.005 MHz
Damping Factor	0.2425
Natural Frequency	305.045 kHz
PSD of Noise	-89.4322 dBc/Hz
Lock Range	l 47.9524 kHz
Lock-in Time	3.278 µs
Pull-out Range	682.238 kHz
Pull-in Time	0.6924 µs
Noise Bandwidth	194.222 kHz

Summary of typical parameters from the second order PLL analyzed in the above figures. Results do not reflect operation limits.



Shows the Bode Plot that provides information about the stability of the feedback loop and phase margin. This figure shows the open loop transfer function magnitude (top plot) and the phase of the frequency response (bottom plot).



The poles and zeros plot provides information about the stability and relative value of damping factor and natural frequency of the PLL. The poles (x) are in the left half of the plane indicating a stable PLL.



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