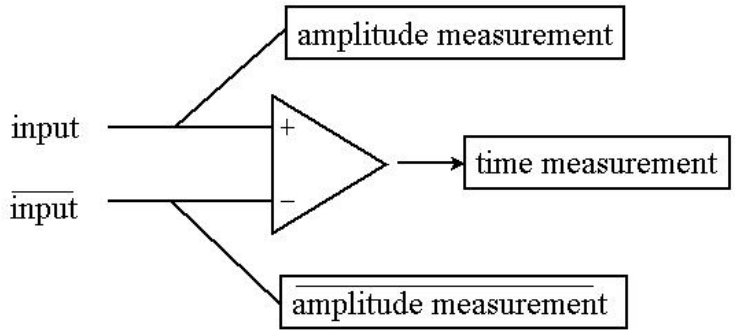
A13 Channel Card Performance Specifications

The A13 channel card is only available in the SIA-3000S product. The A13 channel card has a twin-engine design that includes the functionality of both a sampling oscilloscope and a time interval analyzer. The figure below shows that for each channel card input there is a sampling scope for amplitude measurements and a time interval analyzer used for timing measurements. Section I describes the performance specifications of the timing engine and Section II describes the performance specifications of the amplitude engine.



Block diagram for the channel card inputs

Section I: Timing Engine Performance

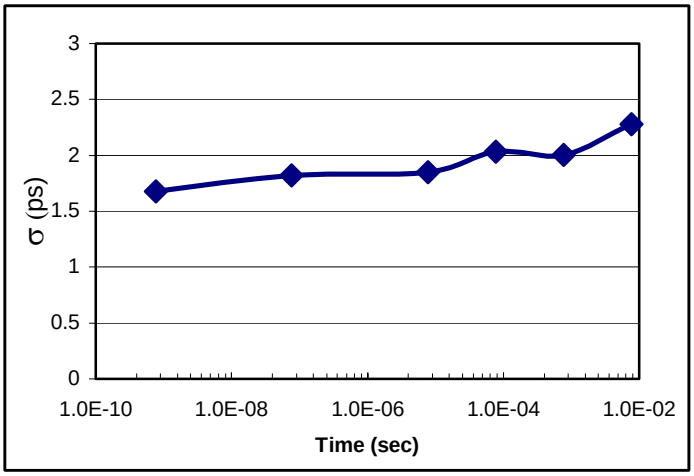
Clock Jitter

The stable time base of the SIA-3000 provides the ability to perform time interval measurements over a broad time span without a significant increase in the wideband jitter noise floor. The frequency range for jitter measurements is 0.4 Hz – 1.3 GHz.

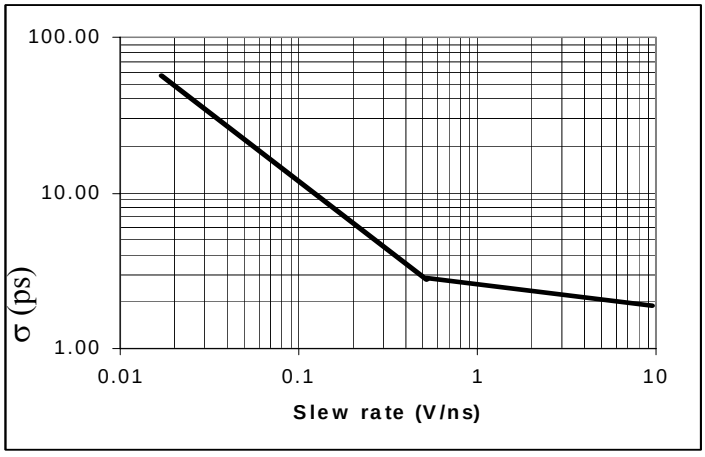
Data in Plot 1 was acquired with a 1.3 GHz, sine wave. Plot 1 shows the σ (standard deviation) of a histogram with 10,000 hits for time intervals ranging from 769 ps (1 period) to 7.69 ms (10,000,000) periods.

The guaranteed noise floor specification, is < 3 ps rms (2 ps typical) for a 1,000 sample period measurement with 1.0 V_{pp}, 0.500–6 GHz sine wave input.

Plot 2 shows the typical rms jitter versus slew rate. The plot shows that to maintain a RJ noise floor below 3 ps rms the slew rate must be >0.5 V/ns.

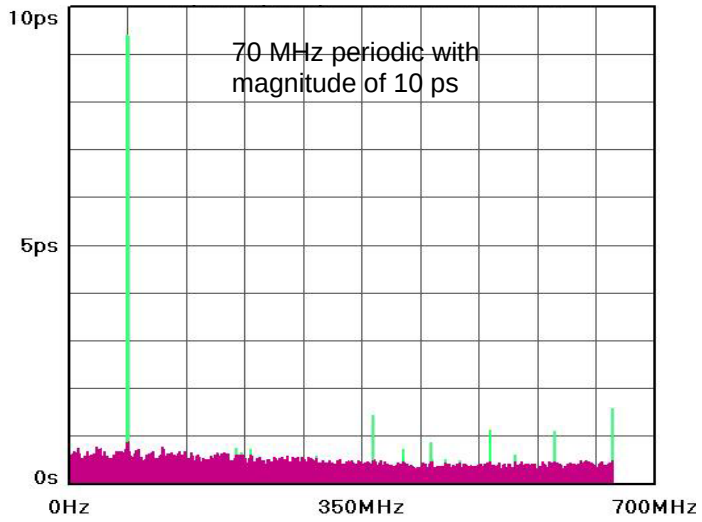


Plot 1



Plot 2

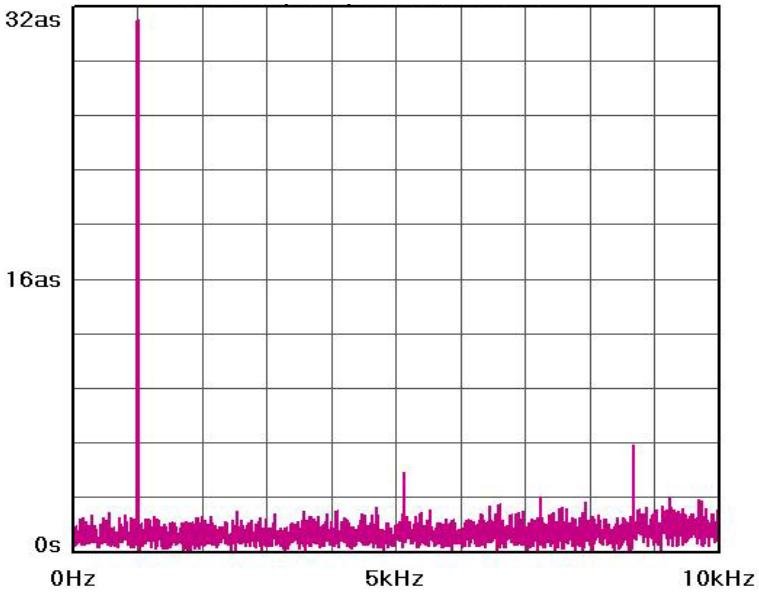
Plot 3 illustrates the capability of the clock analysis tools to isolate periodic components and quantify jitter over a user-defined bandwidth. The plot shows a spectral view of jitter measured from 12 kHz to 650 MHz of a 1.3 GHz sine wave. A 70 MHz sine wave was added to the carrier having a magnitude of 9.5 ps. Post processing filters provide the ability to determine the rms noise over a bandwidth. For example, the typical rms jitter from 12 kHz to 20 MHz is 400 fs determined from this plot.



Plot 3

The Low Frequency Modulation tool provides the capability of measuring low frequency (<100 kHz) periodic components on a carrier. Plot 4 shows the spectral view of jitter over 1 clock period from 0 Hz to 10 kHz of a 1.3 GHz sinewave modulated with a 50 Hz peak deviation 1 kHz sinewave. The 1 kHz spectral component has a magnitude of 31 as and the background noise is <1 as.

NOTE: 1 attosecond (as) equals 10^{-18} sec.



Plot 4

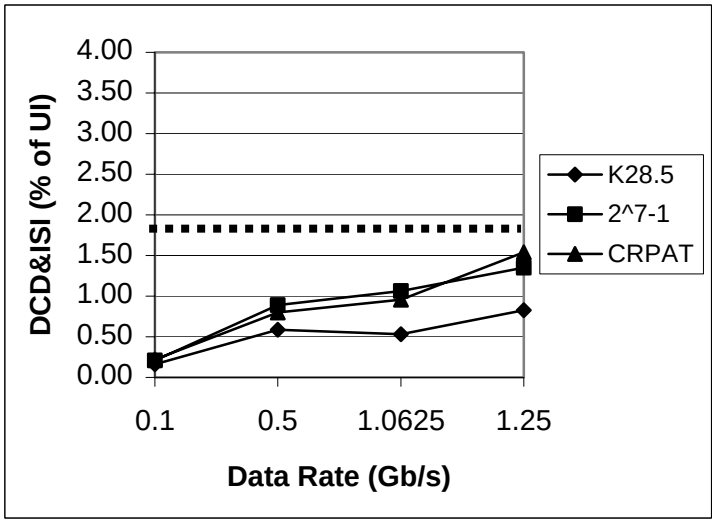
Data Jitter

Data Rate Range ..... up to 1.3 Gb/s

DCD&ISI ..... < 3% UI using CRPAT as the test pattern

RJ ..... 800 fs typical across the bandwidth from the Nyquist of the bitrate to bitrate/1667

Plot 5 shows typical instrumentation DCD&ISI performance at various data rates and data patterns. The dashed line represents the guaranteed DCD&ISI specification limit tested at 1.0625 and 1.25 Gb/s. DCD&ISI measurements include the contributions from the pattern generator and cables.



Plot 5

Internal Timebase Reference

Frequency ..... 10 MHz
Aging/year (after 24 hrs on) ..... 1.5×10^{-7}
Aging/day (after 24 hrs on) ..... 1×10^{-9}
Short term (1 sec) stability ..... 5×10^{-11}
(after 1 hr on)

Voltage Performance

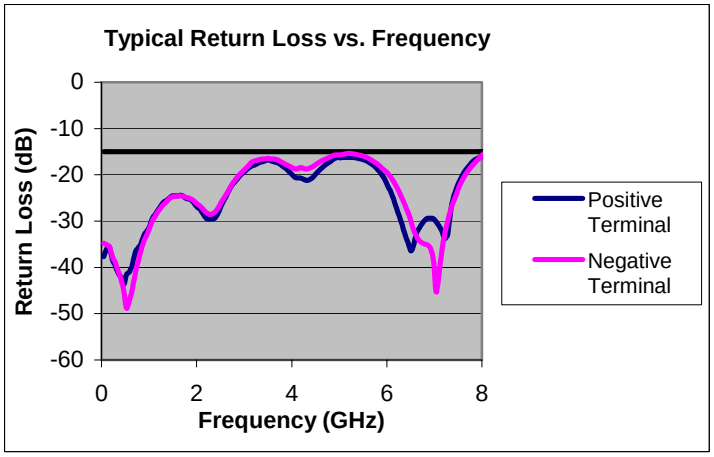
Input voltage range ..... ±1.5 V

The Input Voltage Range is defined as the minimum and maximum input voltage levels, relative to chassis ground, that the inputs can safely accept and meet performance specifications.

Electrical Input ..... Female SMA

Input Sensitivity ..... 50 mV_{pp} differential
100 mV_{pp} single-ended

Return Loss ..... With respect to 50Ω less than –15 dB from 10 MHz to 6 GHz as shown in plot 6.



Plot 6

Timing Engine Standard Measurements/Features

Random Jitter, Deterministic Jitter, DCD&ISI, BER, Periodic Jitter, Skew, Propagation Delay, Period Jitter, Pulse Width Jitter, Cycle-to-Cycle Jitter, RMS Jitter over a bandwidth, Duty Cycle, Frequency, Damping Factor, Natural Frequency, Lock Range, Lock-in Time, Pull-in Time, Pull-out Range, Noise Bandwidth, PSD of Noise, Poles and Zeros.

Section II: Amplitude Engine Performance

Each input to the A13 channel card has an integrated sampling oscilloscope to provide accurate and repeatable amplitude measurements. This section describes the performance characteristics of amplitude engine.

Analog Bandwidth (-3 dB) ..... >6 GHz

Rise Time ..... 60 ps (10% to 90%, calculated from RT=0.35/BW)

DC Voltage Accuracy ..... +/-(5mV + 0.5% × offset voltage)

Input Dynamic Range ..... 1 V_{pp} (Single-ended)

RMS Noise ..... <4 mV

Horizontal System

Delay

Minimum..... >24ns
Maximum..... 100 μs

Oscilloscope timebase jitter (rms)* .... <1 ps + 10 ppm of delay setting
*Any additional trigger error will increase this value

Timebase Delay Accuracy..... <8 ps + 0.1% of delay

Time Interval Resolution..... 300 fs

Vertical System

Vertical Resolution ..... 300 μV

Trigger Modes

Self Trigger (for clock patterns only up to 6 GHz)
External Trigger (up to 6 GHz)
Internal Pattern Trigger: Directly connected from PM50

Amplitude Engine Standard Measurements/Features

Rise Time, Fall Time, Overshoot, Undershoot, V_{max}, V_{mid}, V_{min}, V_{top}, V_{base}, V_{pk-pk}, V_{amp}, V_{RMS}, V_{AVG}
Mask Violations, Mask Comparisons, Horizontal and Vertical histograms and statistics.

Note: Typical measurements provide non-warranted information about system performance or capabilities.